

INTEL(R) CELERON(TM) PROCESSOR (PPGA)/INTEL(R) 810 CHIPSET UNIPROCESSOR CUSTOMER REFERENCE SCHEMATICS REVISION 1.3

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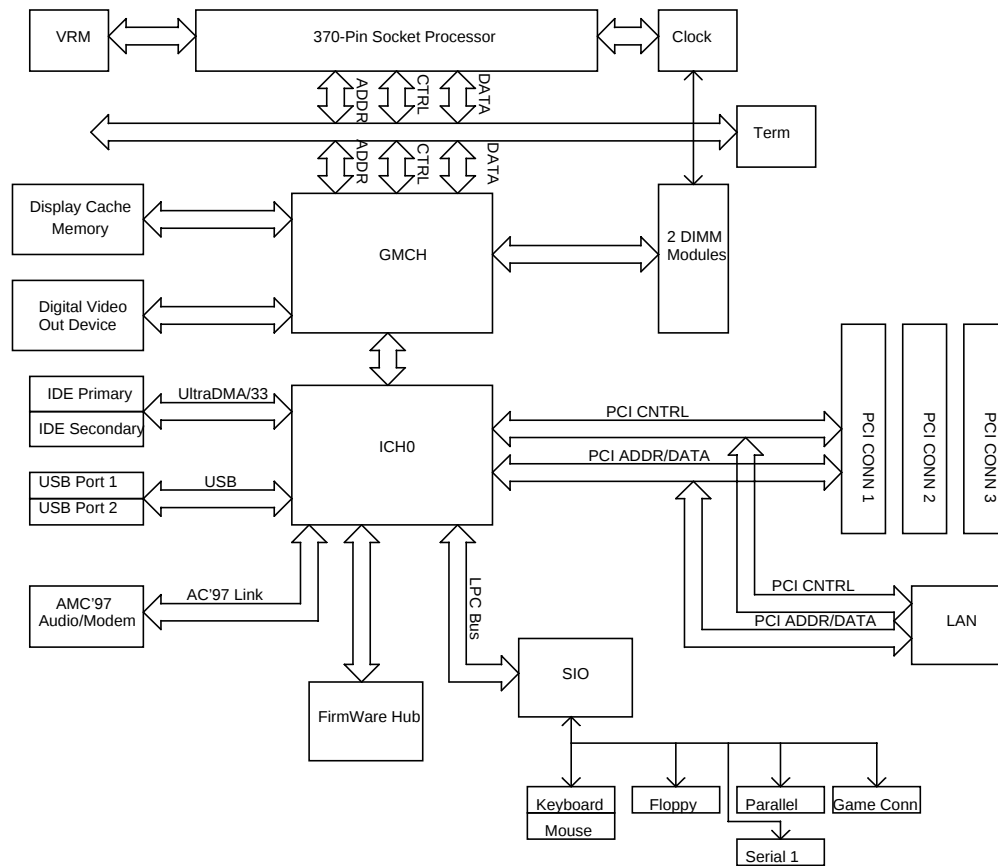
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Block Diagram



Device Table

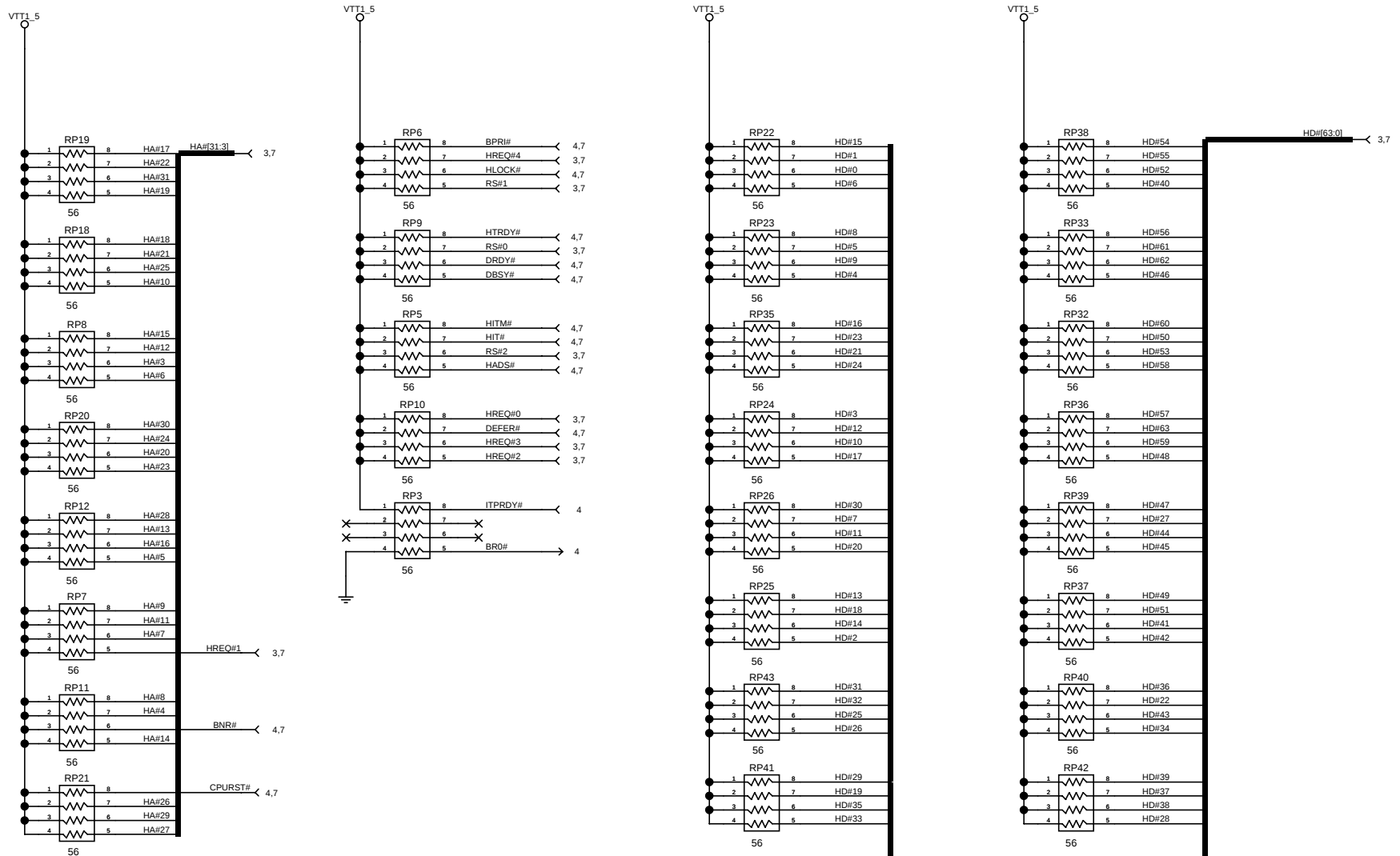
REFERENCE DESIGNATOR	DEVICE TYPE	GATES USED	SHEET NUMBER
U12	74lvc14a	A,B,C,D	32
U16,U17	gd75232		22
U15	lpc47b27_a		16
U3	74lvc06a	A,B,C,D	29,32
U1	ck-whitney		6
U2	82810-DC100		7,8,9
U14	82801AB		13,14
U7	sii-dfp		24
U13	82559		27
U8,U9	1x16sdram		10
U10	74lvc08a	A,B	32
U6	qst3384		25
U18	93c46		27
U4	74ls132	A,B	29,32
U5	74lvc07a	A,B,C	29,31
U11	74lvc07a	A,B,C	19,31
VR2,VR3	lt1587ad		29
VR4	lt1117_3		29
VR1	ltc1753		30
VR5	lt1585ad		29

370PGA Socket
Part 1

370-Pin Socket
Part 1

TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD		REV: 1.3
370-PIN SOCKET, PART 1		
	PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 11-23-1998 13:44
	PROJECT: INTEL(R) 810 CHIPSET SHEET: 3 OF 40	

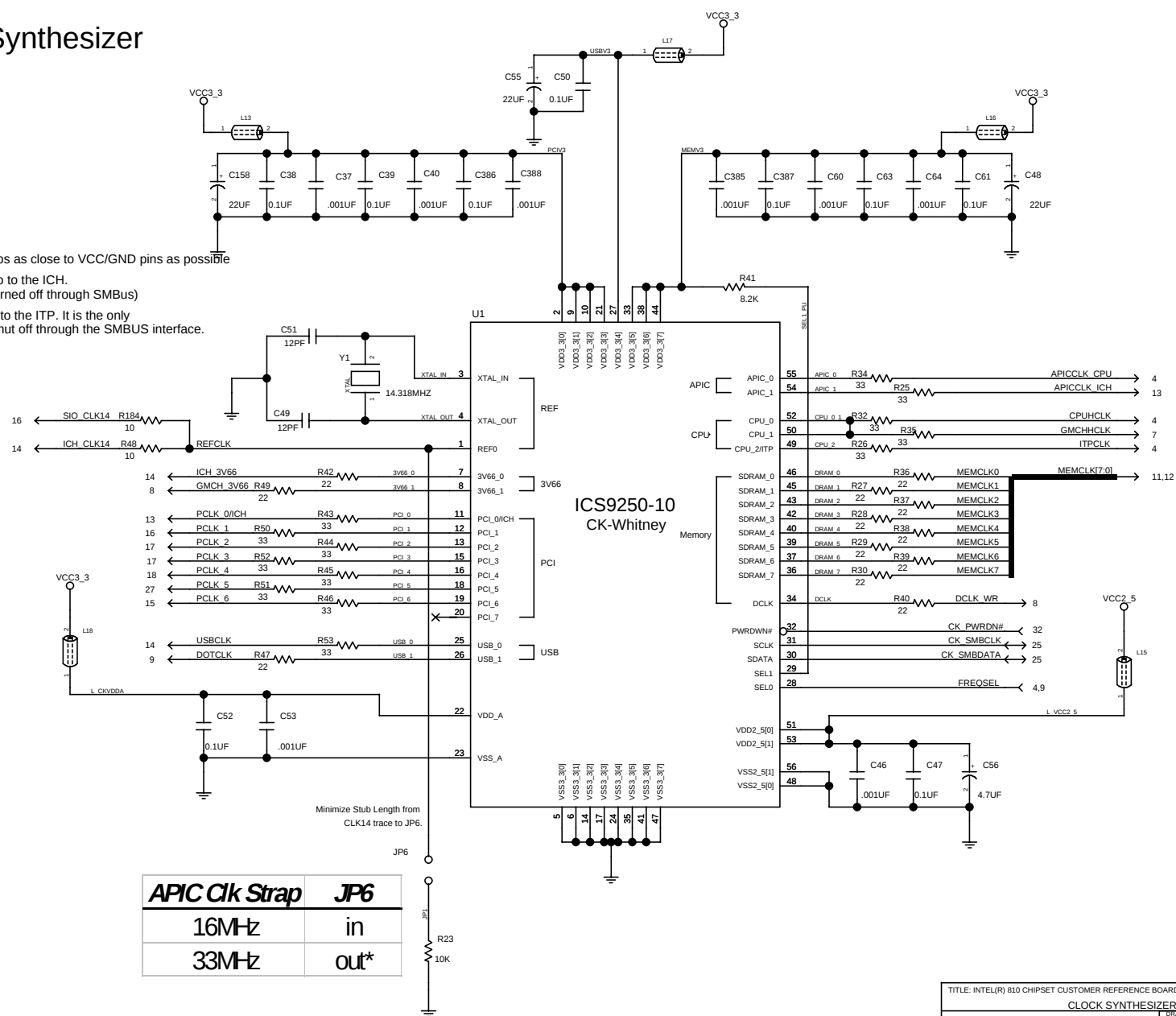
GTL Termination



Clock Synthesizer

Notes:

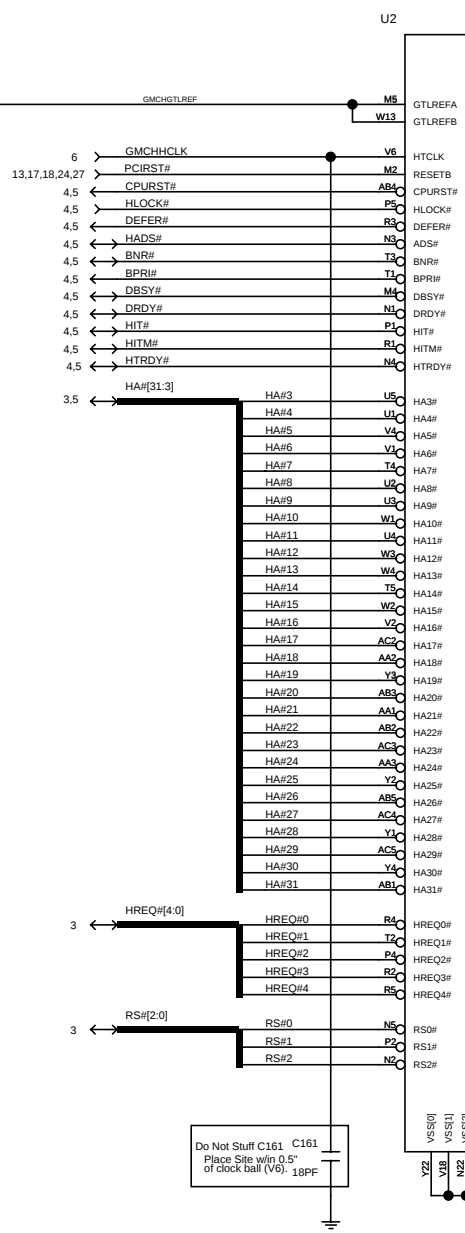
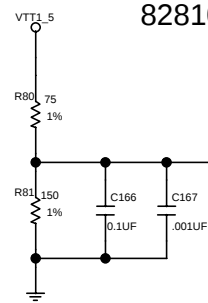
- Place all decoupling caps as close to VCC/GND pins as possible
- PCI_O/ICH pin has to go to the ICH.
(This clock cannot be turned off through SMBus)
- CPU_IPT pin has to go to the ITP. It is the only CPU CLK that can be shut off through the SMBUS interface.



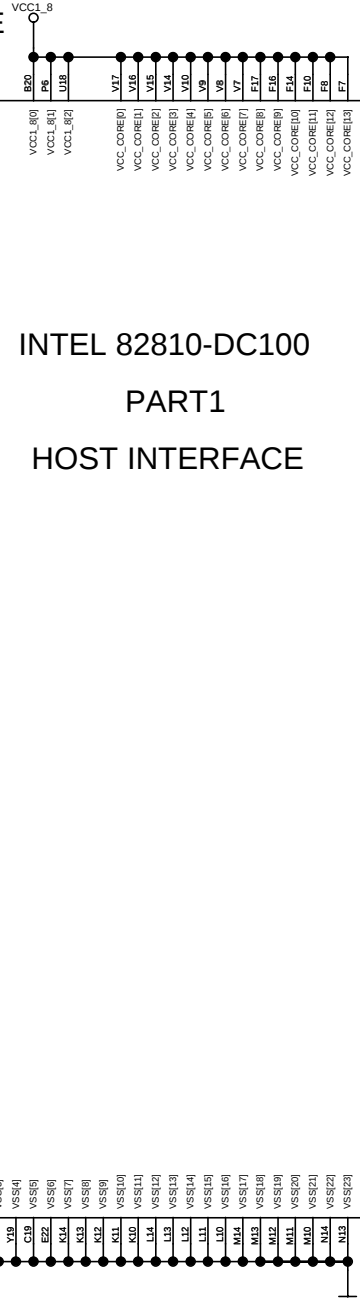
<i>APIC Clk Strap</i>	<i>JP6</i>
16MHz	in
33MHz	out*

82810-DC100, PART 1: HOST INTERFACE

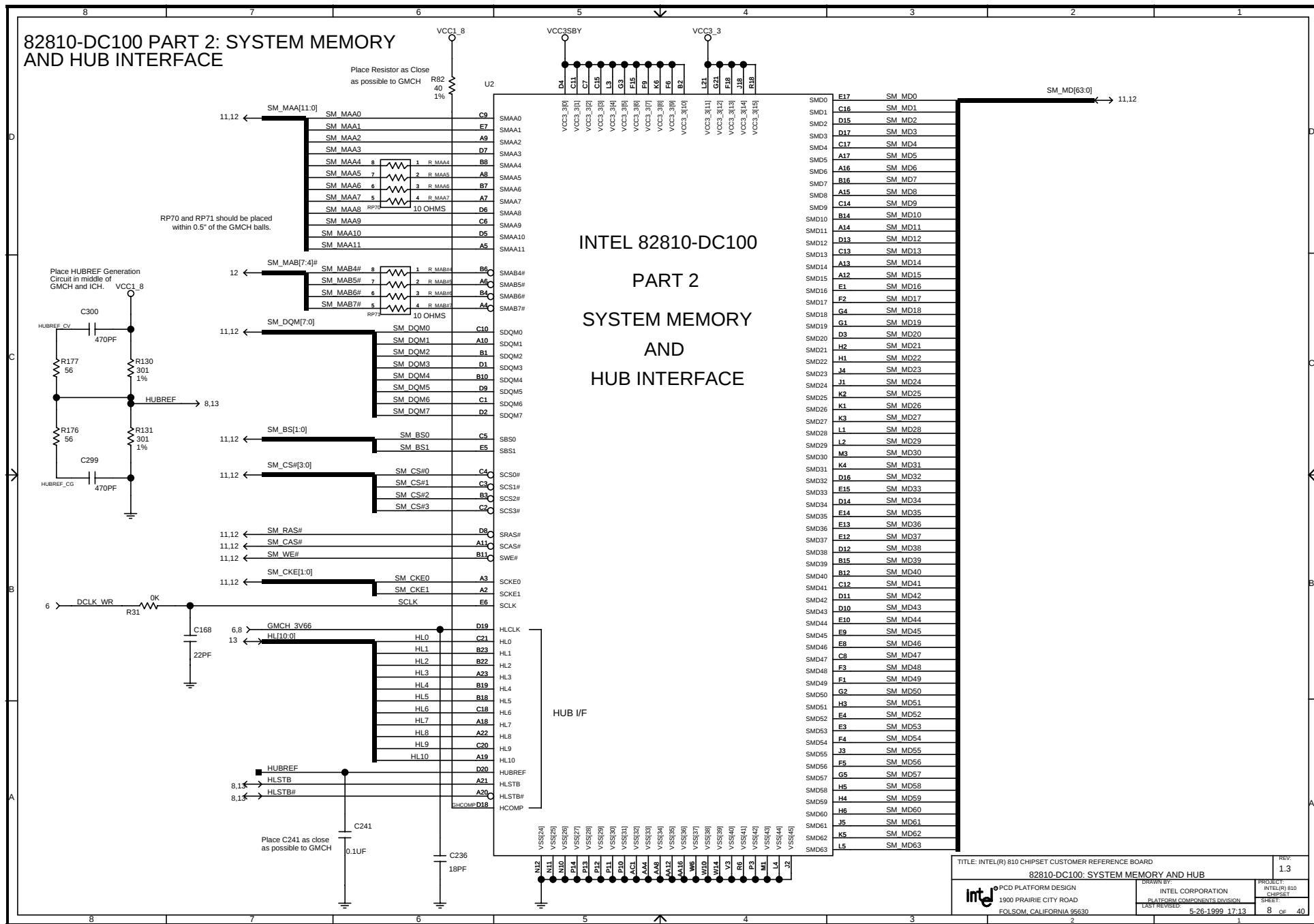
INTEL 82810-DC100 PART1 HOST INTERFACE



Do Not Stuff C161 C161
Place Site win 0.5"
of clock ball (V6). 18PF

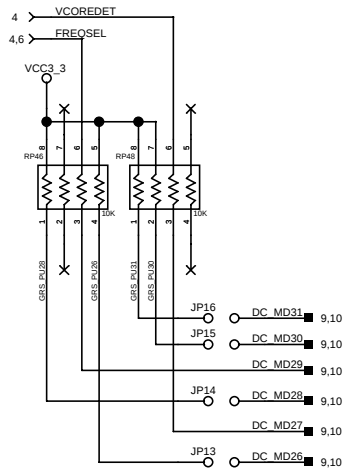


HD0#	Y5	HD#0
HD1#	W5	HD#1
HD2#	W8	HD#2
HD3#	AA6	HD#3
HD4#	AB6	HD#4
HD5#	Y6	HD#5
HD6#	AA5	HD#6
HD7#	AA9	HD#7
HD8#	Y5	HD#8
HD9#	AC7	HD#9
HD10#	AB7	HD#10
HD11#	AC8	HD#11
HD12#	AA7	HD#12
HD13#	Y8	HD#13
HD14#	W7	HD#14
HD15#	AC6	HD#15
HD16#	W9	HD#16
HD17#	AC9	HD#17
HD18#	Y7	HD#18
HD19#	AA10	HD#19
HD20#	AB8	HD#20
HD21#	AC10	HD#21
HD22#	AB13	HD#22
HD23#	AB10	HD#23
HD24#	AB9	HD#24
HD25#	AB11	HD#25
HD26#	Y10	HD#26
HD27#	AB16	HD#27
HD28#	AB12	HD#28
HD29#	Y11	HD#29
HD30#	Y9	HD#30
HD31#	AC12	HD#31
HD32#	W11	HD#32
HD33#	AC11	HD#33
HD34#	W12	HD#34
HD35#	AA11	HD#35
HD36#	AA13	HD#36
HD37#	Y13	HD#37
HD38#	Y12	HD#38
HD39#	AC14	HD#39
HD40#	AA15	HD#40
HD41#	AC15	HD#41
HD42#	Y14	HD#42
HD43#	AC13	HD#43
HD44#	AA14	HD#44
HD45#	AB14	HD#45
HD46#	Y17	HD#46
HD47#	Y15	HD#47
HD48#	AC17	HD#48
HD49#	AC16	HD#49
HD50#	AA18	HD#50
HD51#	AB15	HD#51
HD52#	W15	HD#52
HD53#	AB18	HD#53
HD54#	W17	HD#54
HD55#	AA17	HD#55
HD56#	W18	HD#56
HD57#	W16	HD#57
HD58#	AC19	HD#58
HD59#	Y16	HD#59
HD60#	AB19	HD#60
HD61#	Y18	HD#61
HD62#	AC18	HD#62
HD63#	AB17	HD#63

82810-DC100 PART 2: SYSTEM MEMORY
AND HUB INTERFACE

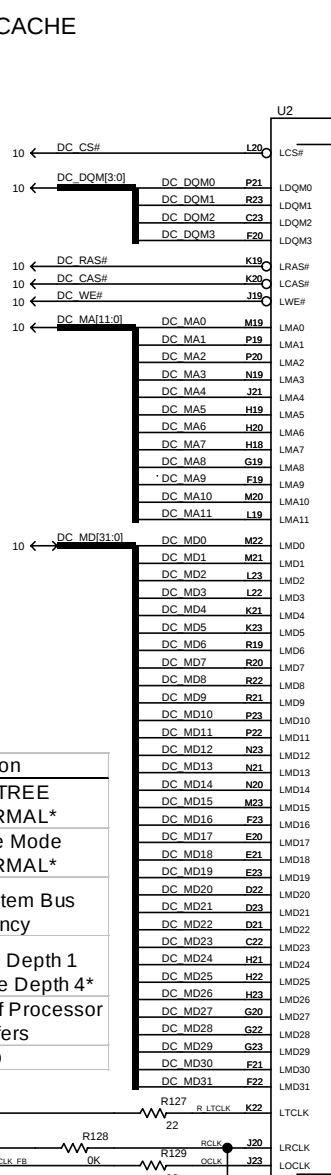
82810-DC100, PART 3: DISPLAY CACHE AND VIDEO INTERFACE

GMCH RESET STRAPS



Function	Jumper	Function
XOR	JP16	IN=XOR TREE OUT=NORMAL*
Tri-State	JP15	IN=TriState Mode OUT=NORMAL*
System Bus Frequency	N/A	READS System Bus Frequency
IOQD	JP14	IN=IO Queue Depth 1 OUT=IO Queue Depth 4*
VCORE Detect	N/A	Detects Type of Processor I/O Buffers
RESVD	JP13	TBD

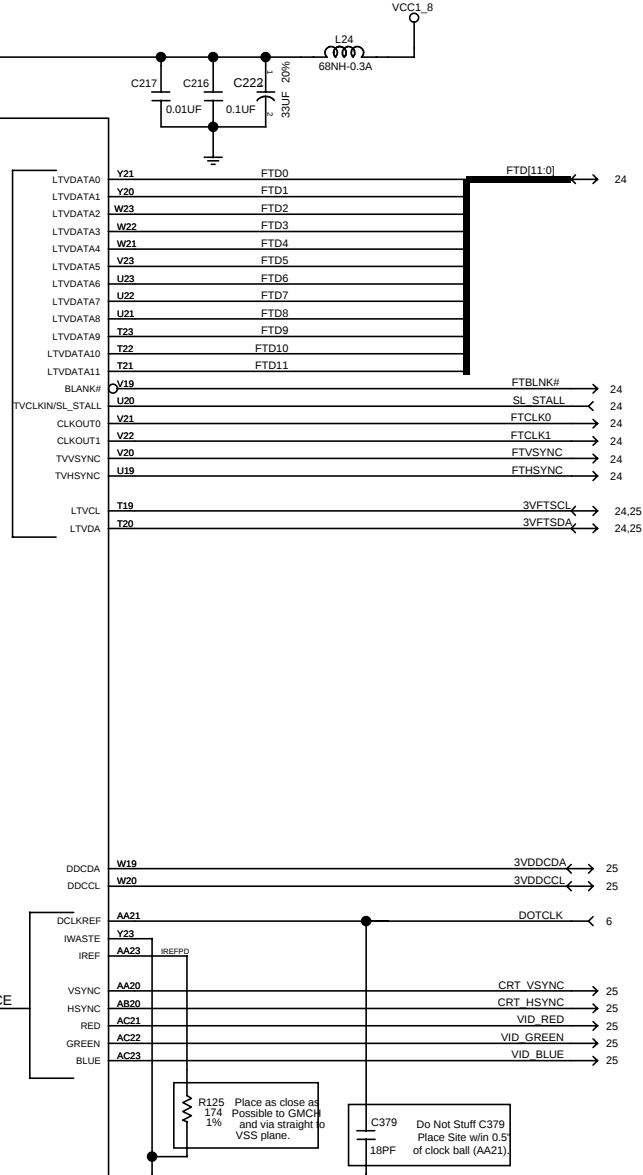
INTEL 82810-DC100 PART 3 DISPLAY CACHE AND VIDEO INTERFACE



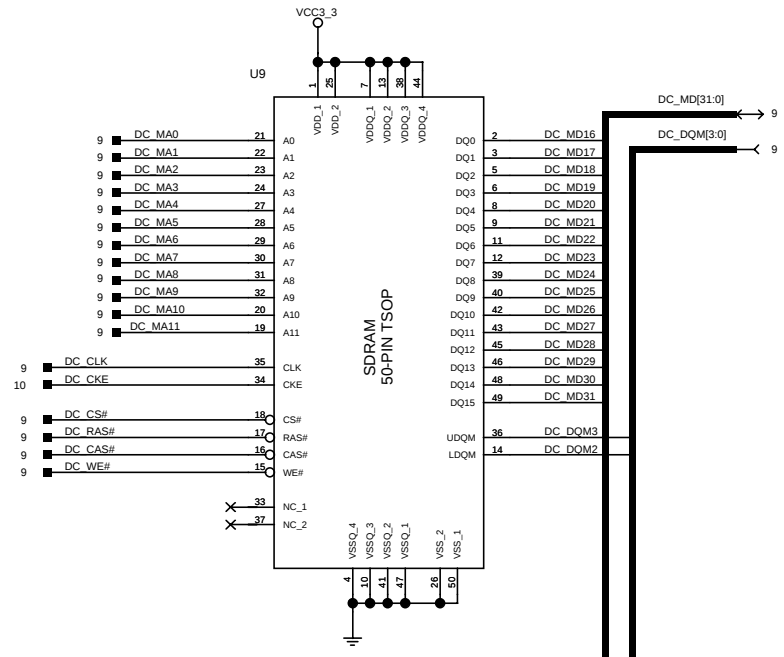
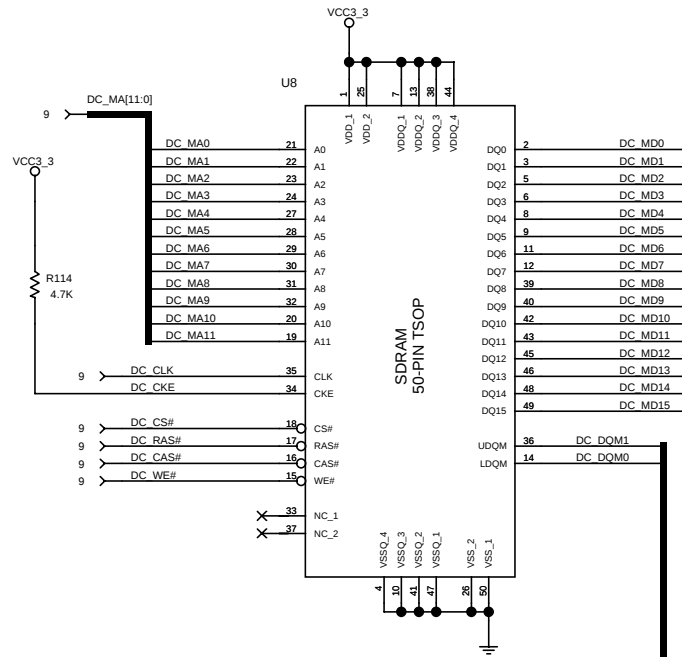
DISPLAY CACHE INTERFACE

VIDEO DIGITAL OUT INTERFACE

GRAPHICS INTERFACE



4MB Display Cache



SYSTEM MEMORY

DIMM0
SLAVE ADDRESS = 1010000B

DIMM SOCKET
168 PIN

Memory Modules: SM MD0, SM MD1, SM MD2, SM MD3, SM MD4, SM MD5, SM MD6, SM MD7, SM MD8, SM MD9, SM MD10, SM MD11, SM MD12, SM MD13, SM MD14, SM MD15, SM MD16, SM MD17, SM MD18, SM MD19, SM MD20, SM MD21, SM MD22, SM MD23, SM MD24, SM MD25, SM MD26, SM MD27, SM MD28, SM MD29, SM MD30, SM MD31, SM MD32, SM MD33, SM MD34, SM MD35, SM MD36, SM MD37, SM MD38, SM MD39, SM MD40, SM MD41, SM MD42, SM MD43, SM MD44, SM MD45, SM MD46, SM MD47, SM MD48, SM MD49, SM MD50, SM MD51, SM MD52, SM MD53, SM MD54, SM MD55, SM MD56, SM MD57, SM MD58, SM MD59, SM MD60, SM MD61, SM MD62, SM MD63.

Memory Banks: SM MA0, SM MA1, SM MA2, SM MA3, SM MA4, SM MA5, SM MA6, SM MA7, SM MA8, SM MA9, SM MA10, SM MA11.

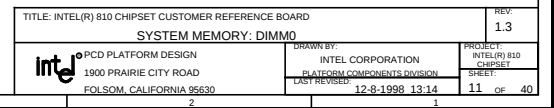
Memory Controllers: SM CS#0, SM CS#1, SM WE#, SM CAS#, SM RAS#, SM CKE1#0.

Control Signals: MEMCLK[7:0], SM_MAA[11:0], SM_BS[1:0], SM_DQM[7:0], SM_CS#[3:0], SM_WE#, SM_CAS#, SM_RAS#, SM_CKE1#0, SMBDATA, SMBCLK.

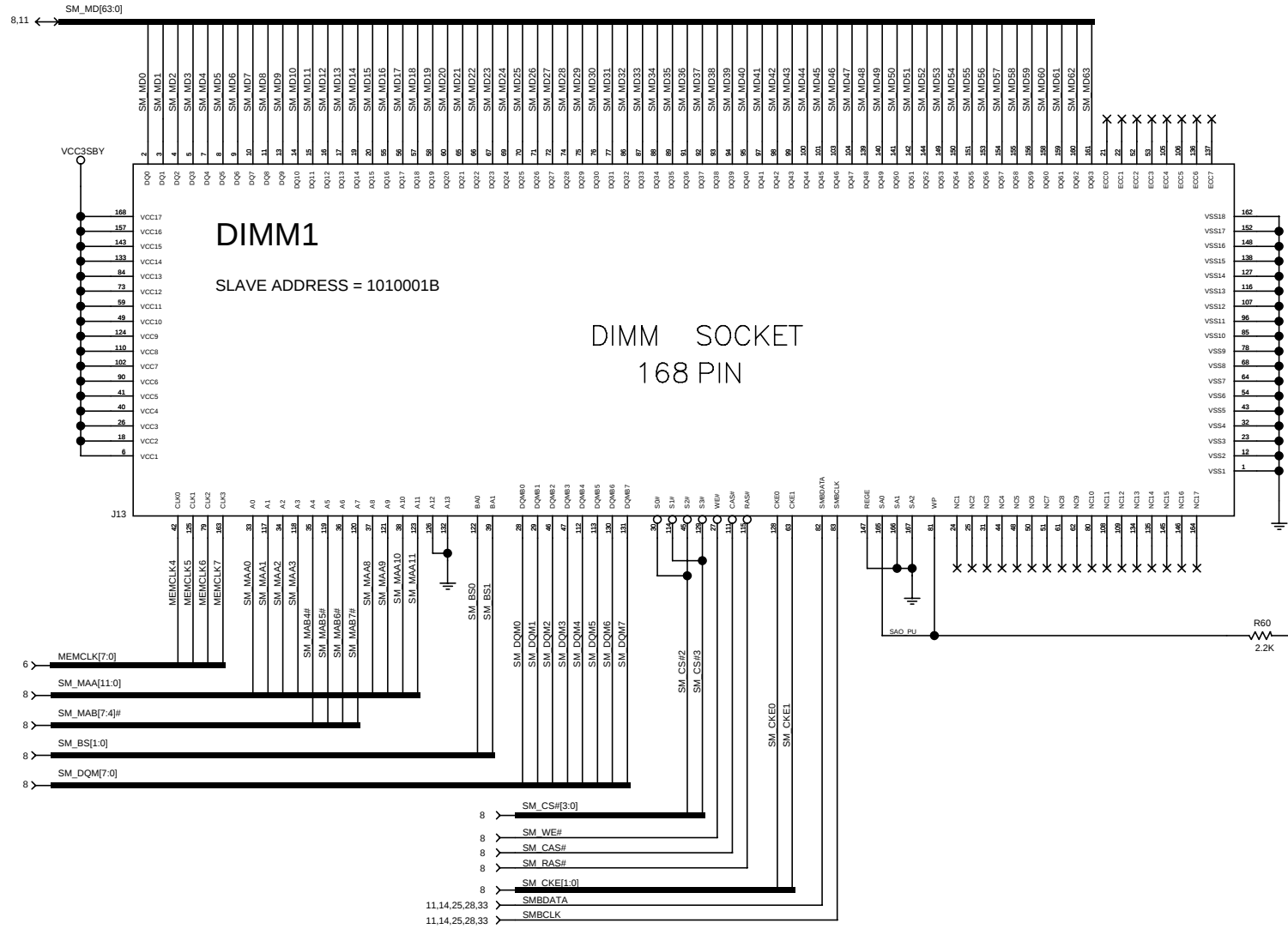
Power and Ground: VCC1-VCC17, VSS1-VSS18, VCC3SBY, SA0 PU.

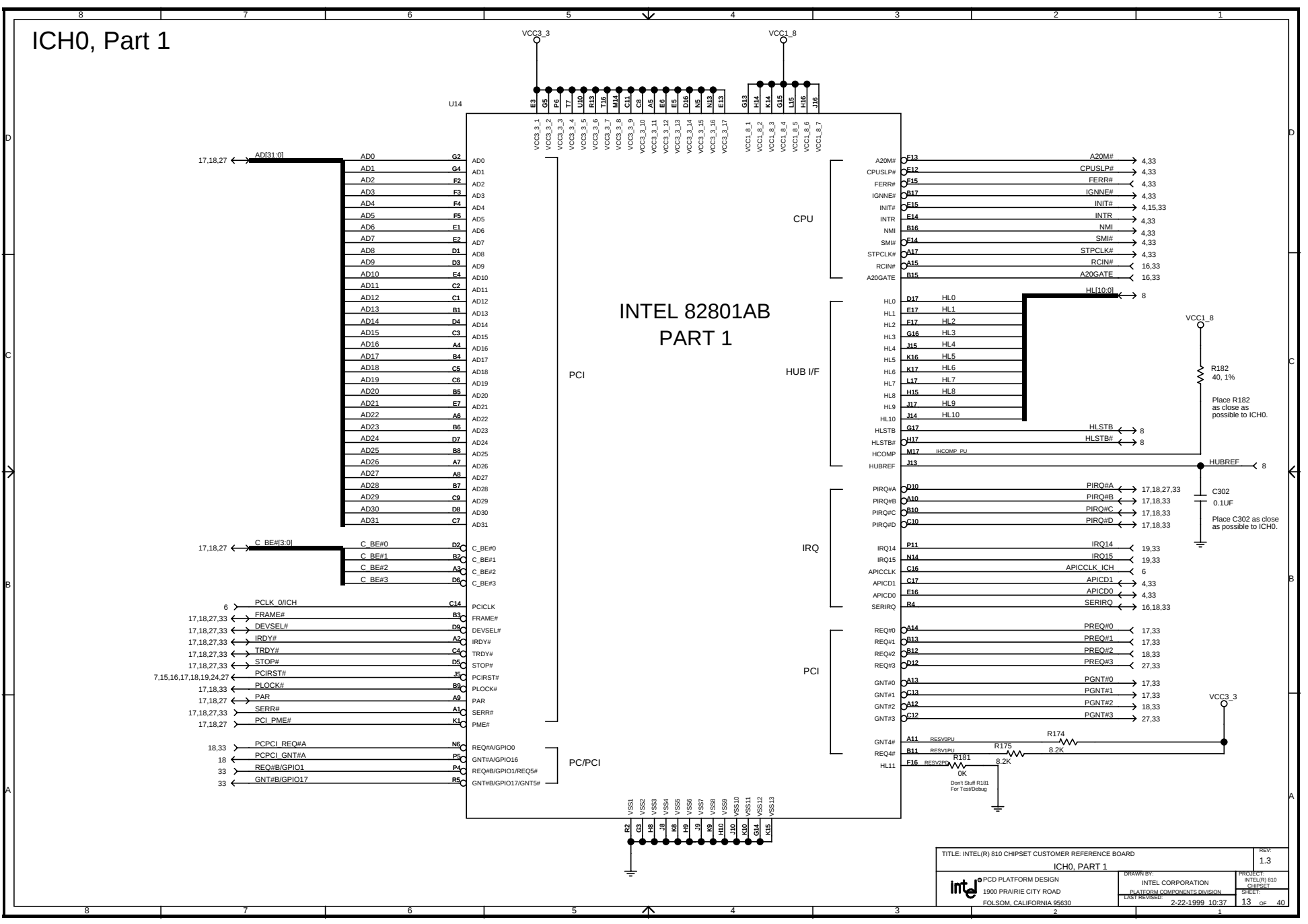
TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD		REV: 1.3
PCD PLATFORM DESIGN		PROJECT: INTEL(R) 810 CHIPSET
1900 PRAIRIE CITY ROAD		SHEET: 11 OF 40
FOLSOM, CALIFORNIA 95630		LAST REVISED: 12-8-1998 13:14

DIMM SOCKET
168 PIN



SYSTEM MEMORY



[illegible]

ICH0 PART 2

JP20 Config	
1-2	Normal
2-3	Clear CMOS

JP17 STRAP (SPKR)	
IN	No Reboot on 2nd watchdog timeout
OUT	Reboot on 2nd watchdog timeout
JP18 (AC_SDOUT)	
IN	Force CPU freq strap to safe mode (1111)
OUT	Use CPU freq strap in ICH register

INTEL 82801AB PART 2

IDE

SYSTEM

AC97

GPIO

LPC

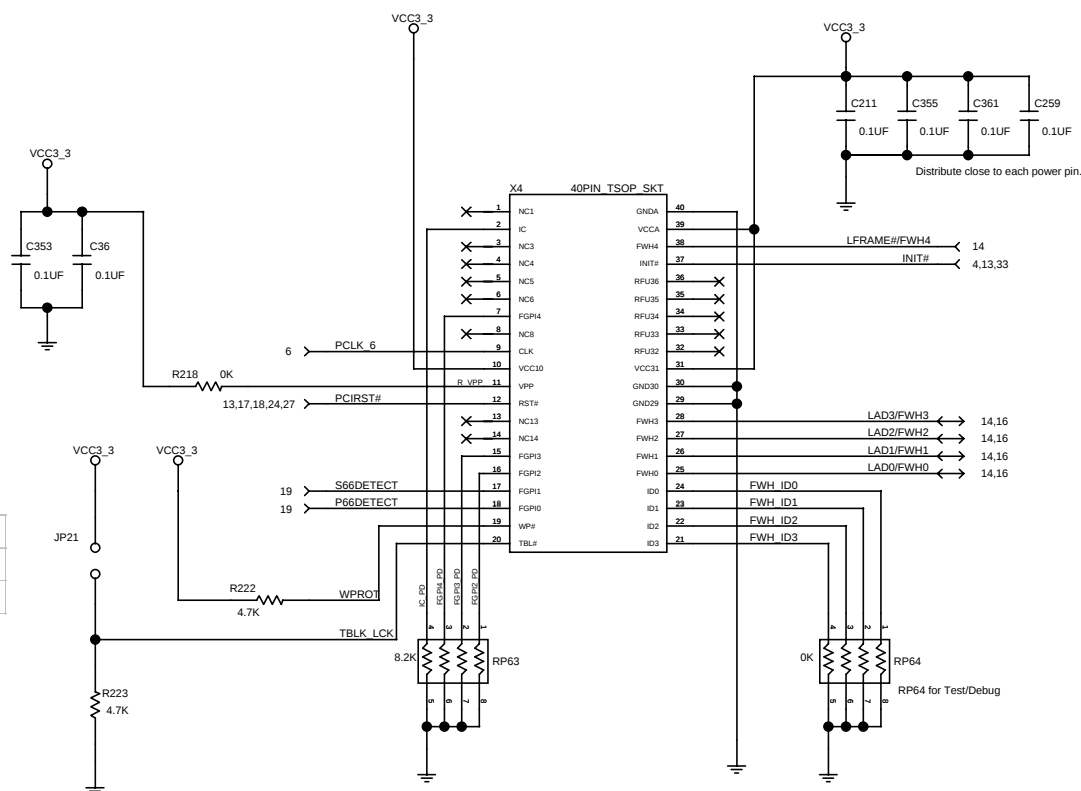
USB

TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD		REV: 1.3
ICH0, PART 2		
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION	PROJECT: INTEL(R) 810 CHIPSET
	PLATFORM COMPONENTS DIVISION	SHEET
	LAST REVISED: 5-26-1999 17:09	14 OF 40

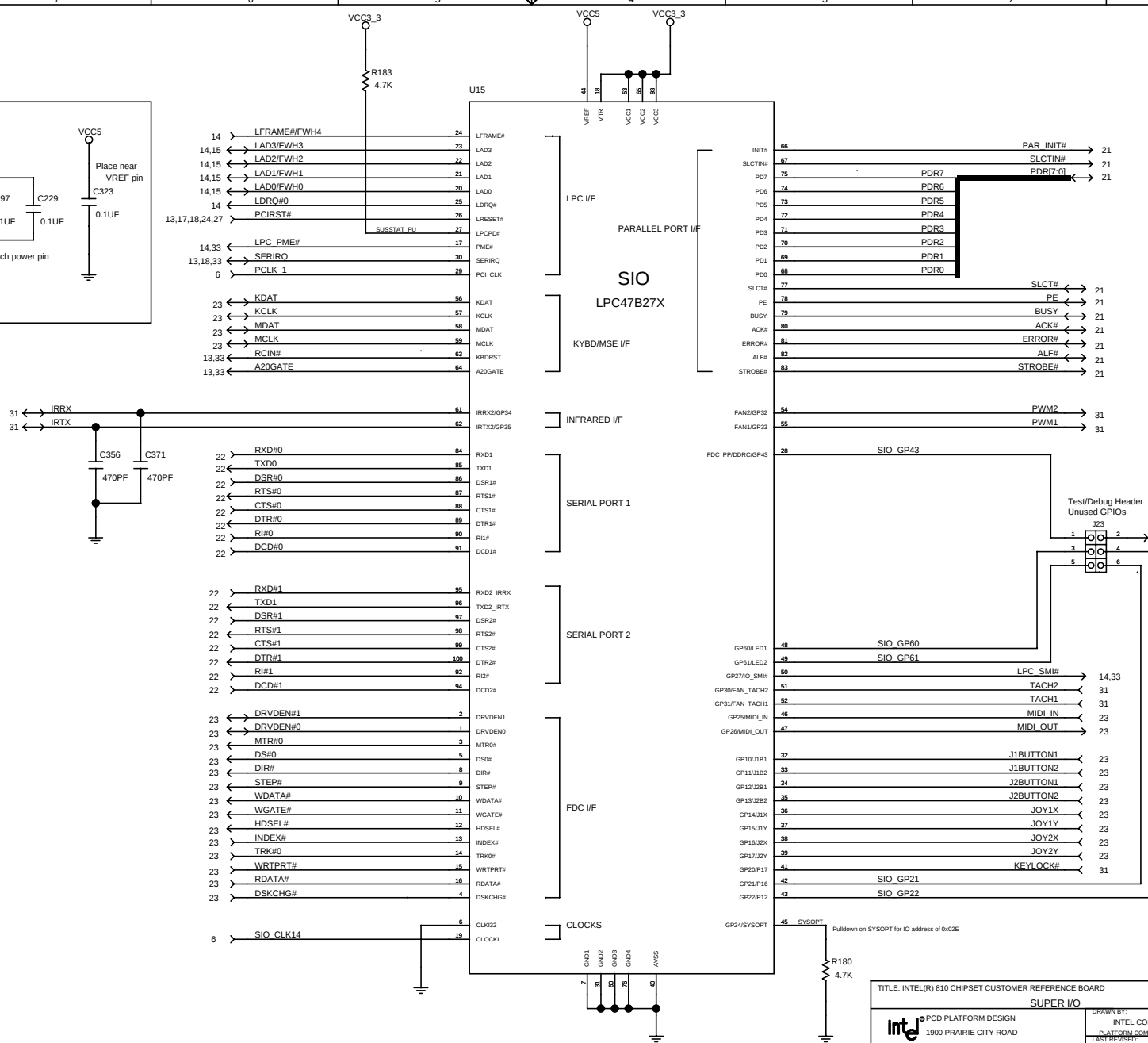
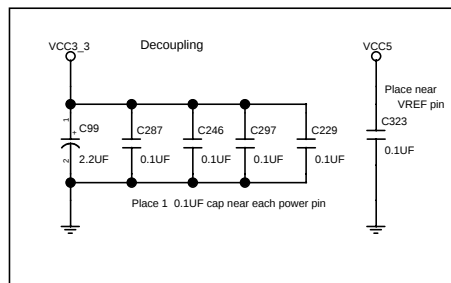
FirmWare Hub (FWH) Socket

NOTE: This is a Socketed Implementation

JP21 CONFIG		
IN	Unlocked	
OUT	Locked	Default

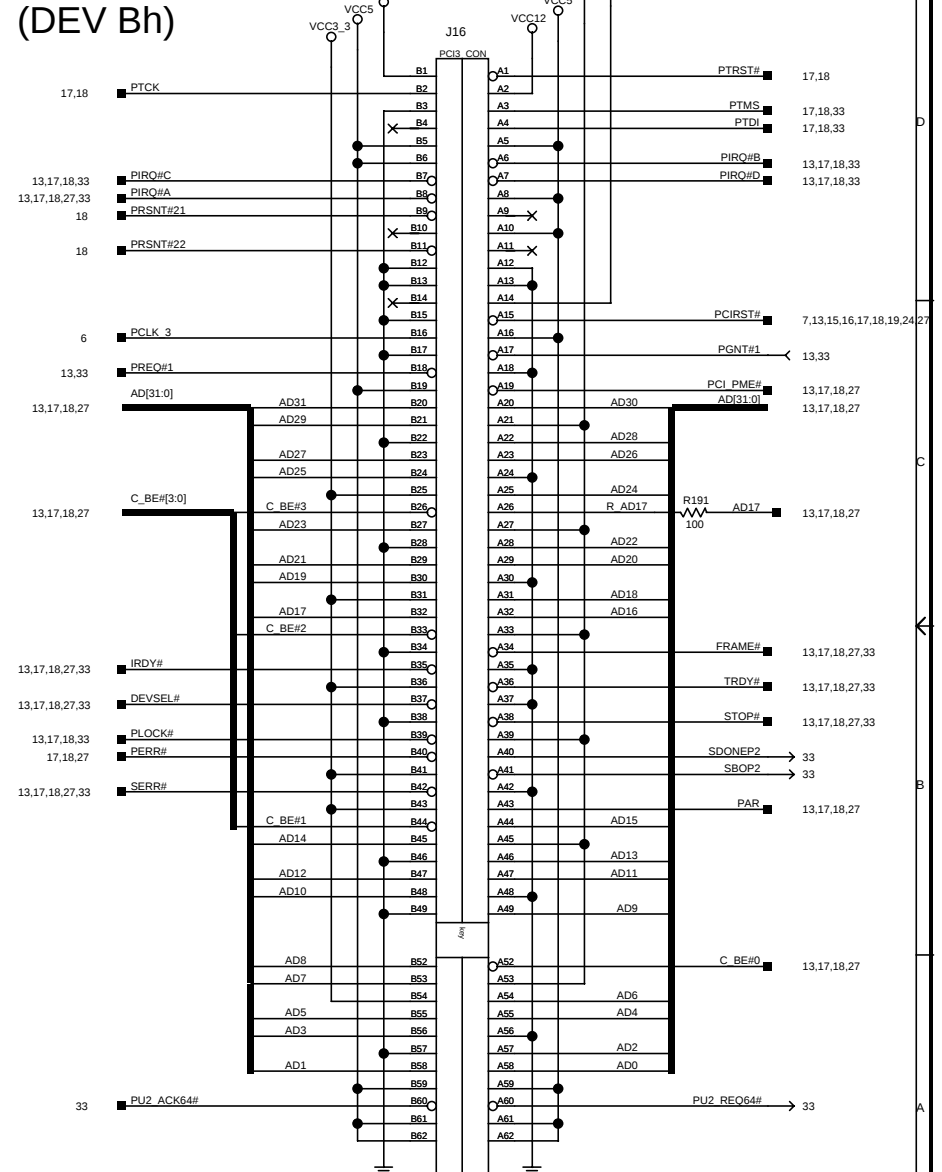
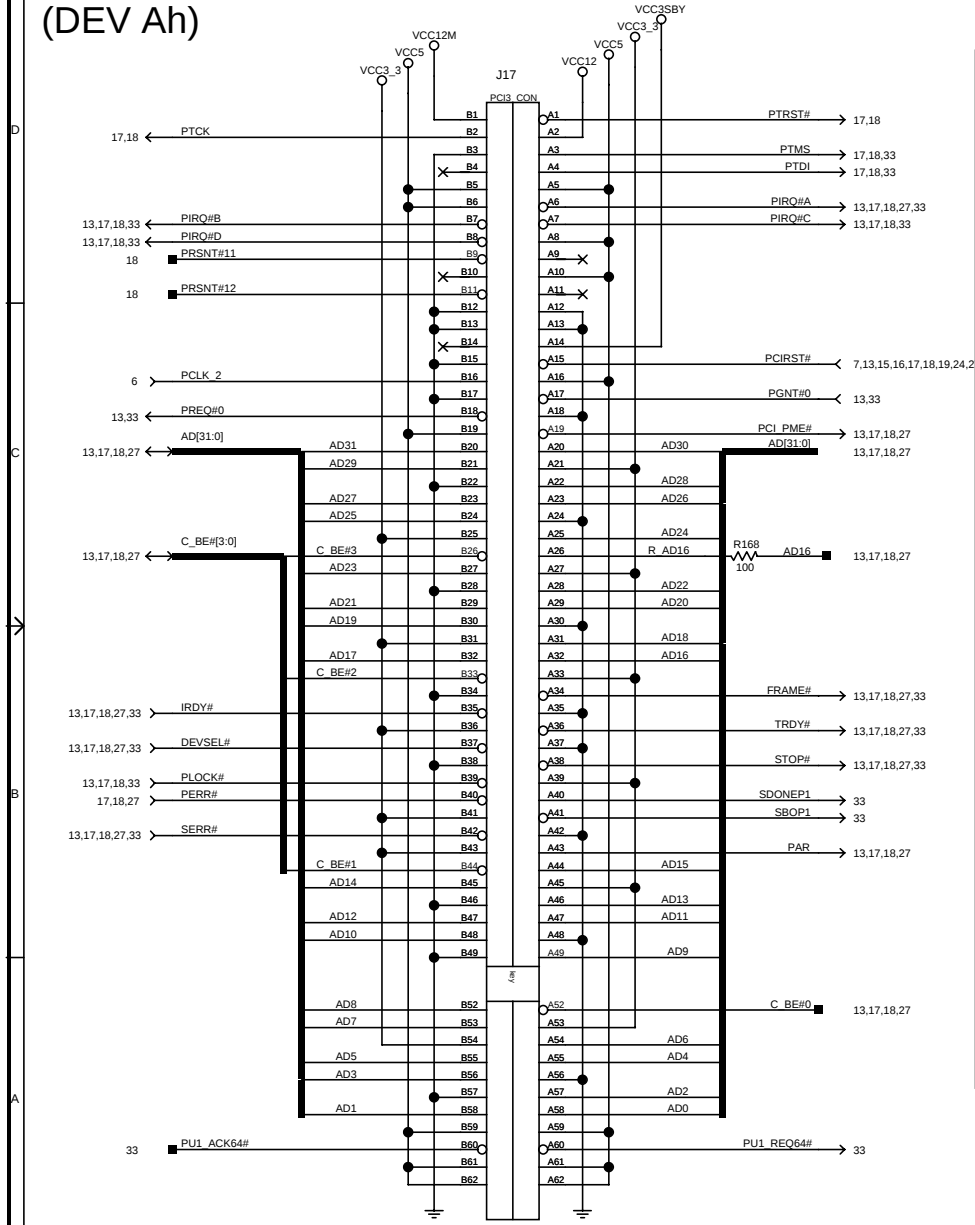


Super I/O



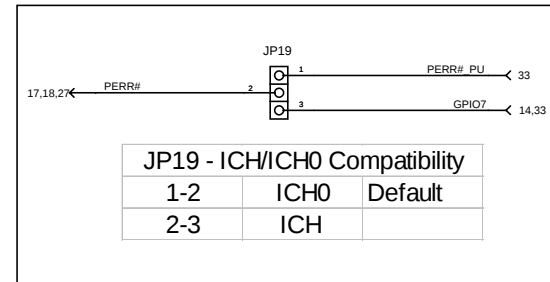
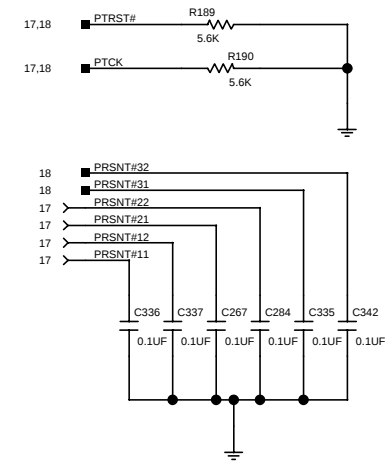
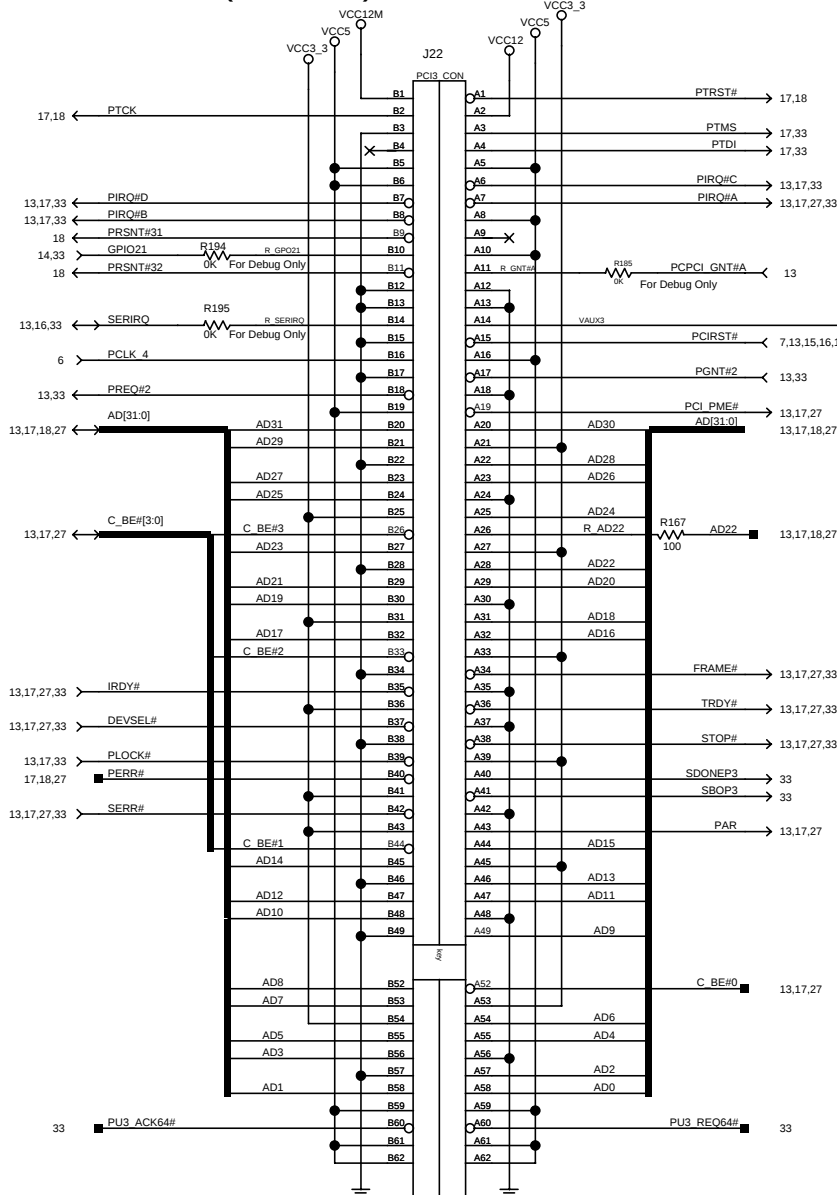
PCI Connector 0 (DEV Ah)

PCI Connector 1 (DEV Bh)

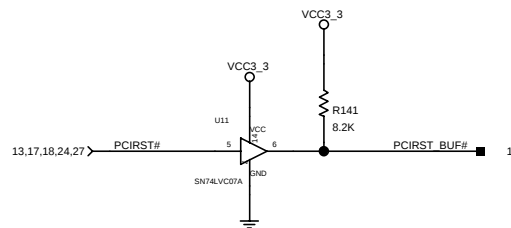
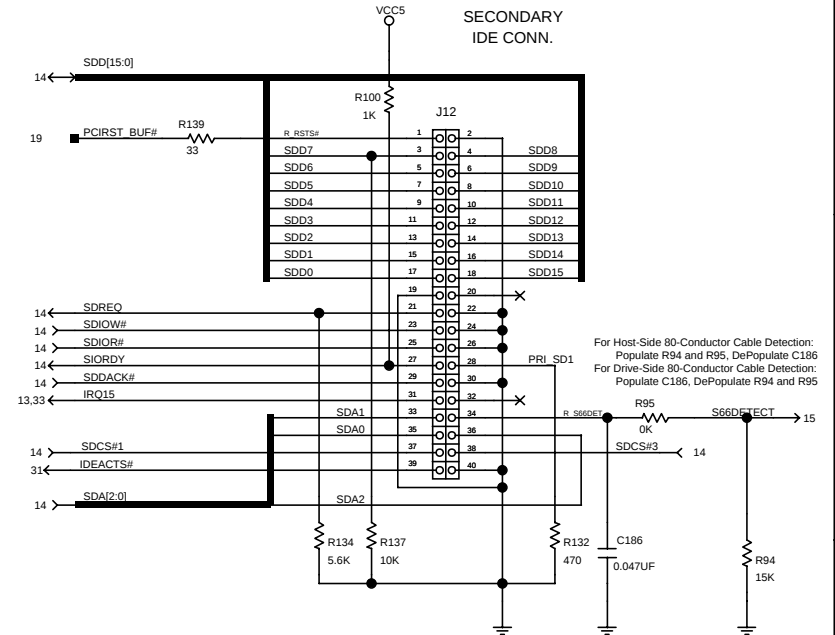
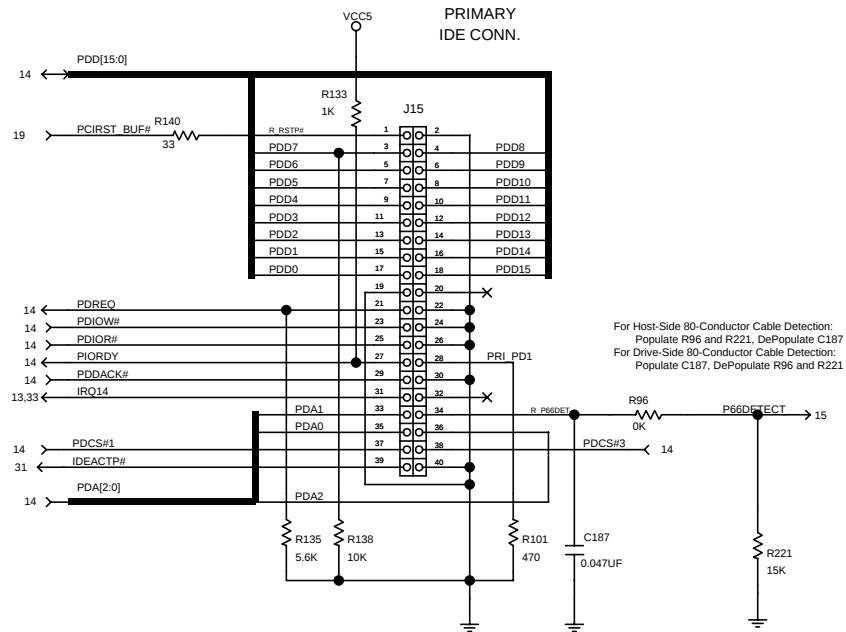


PCI Connector 2 (DEV 6h)

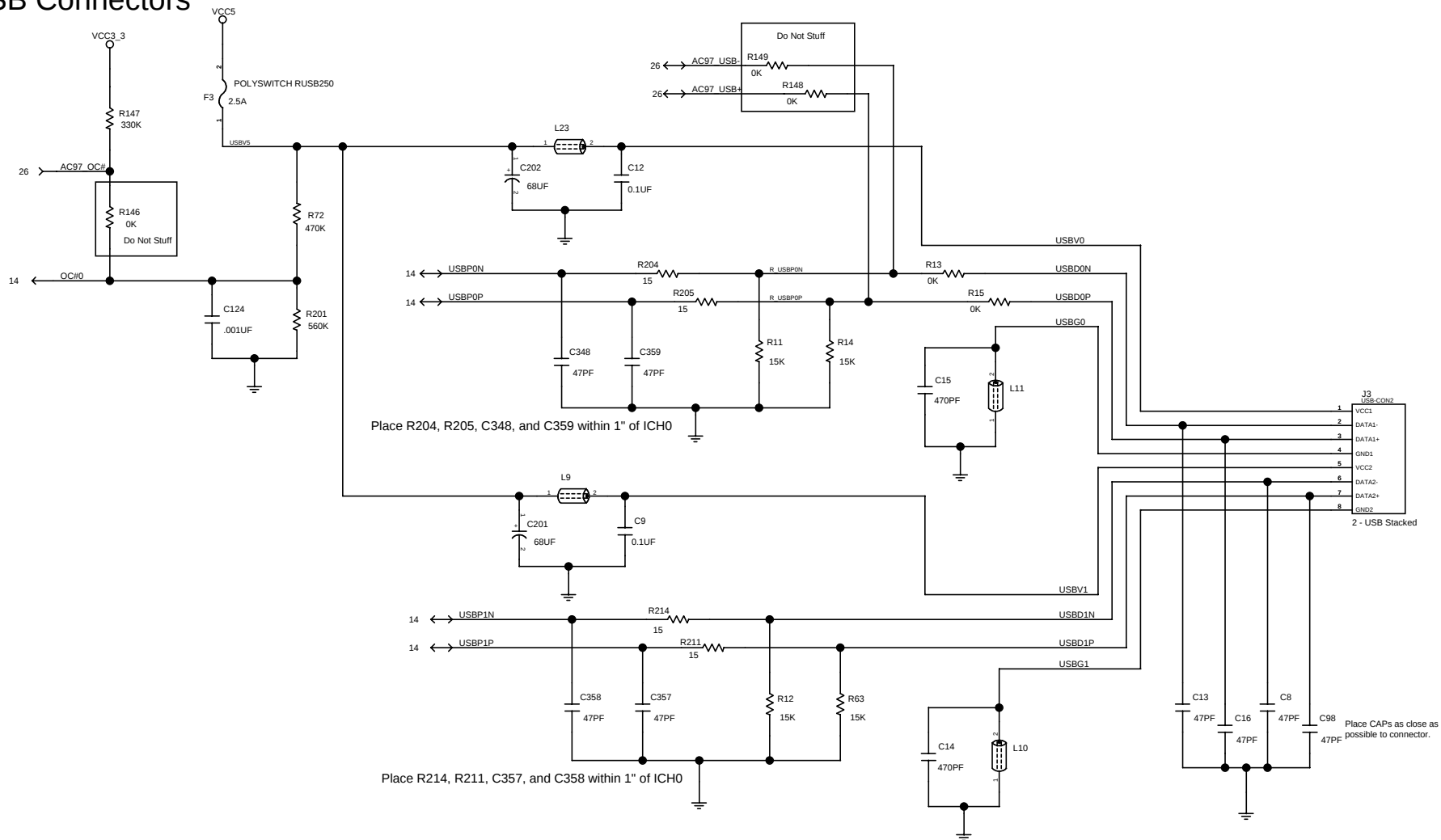
Layout Note: Should be in Slot 0 Position (Outside Edge of Board Furthest from CPU)



ULTRAATA/33 IDE CONNECTORS

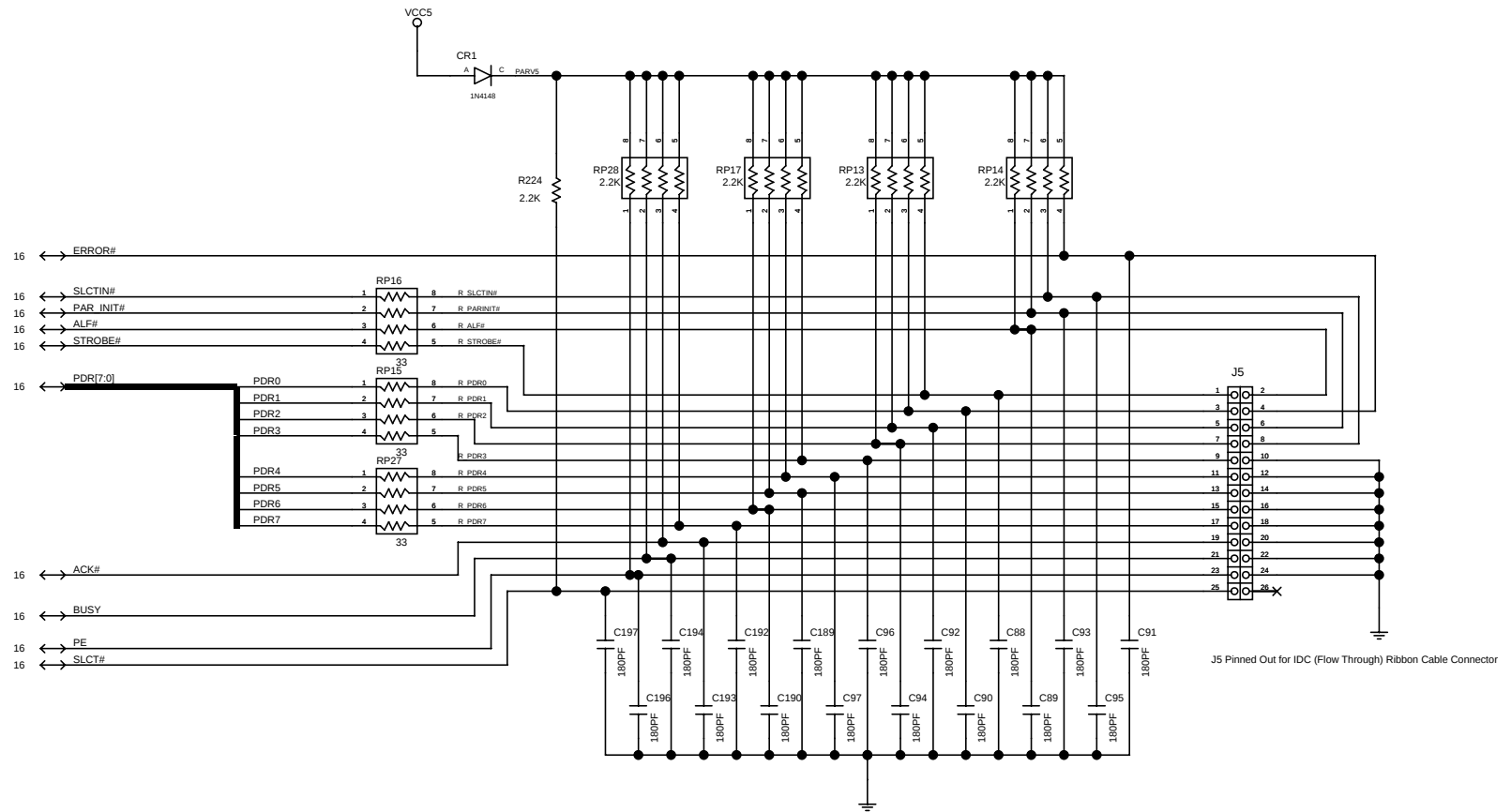


USB Connectors



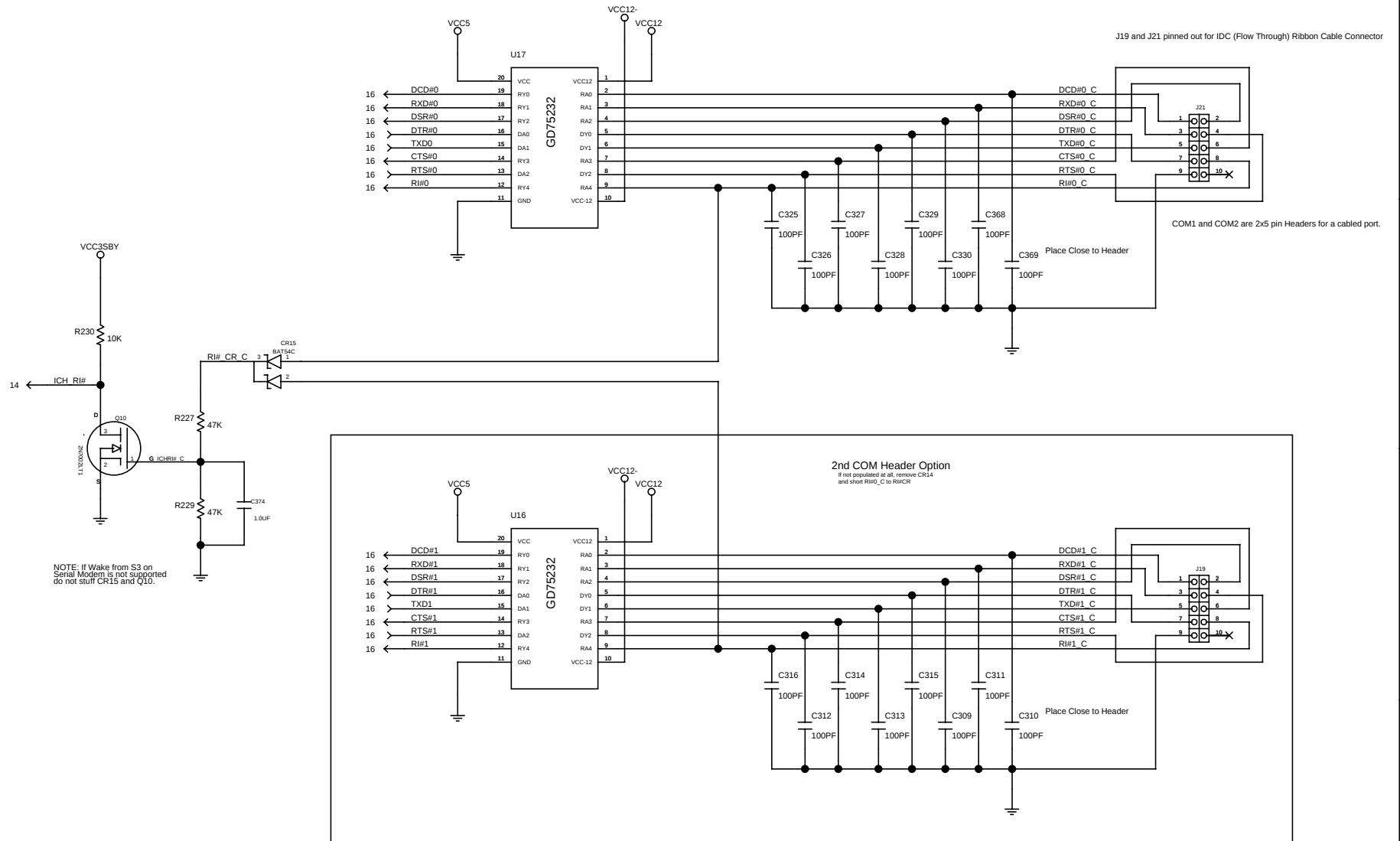
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USB CONNECTORS			
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	PLATFORM COMPONENTS DIVISION	SHEET: 20 OF 40	
	LAST REVISED: 11-23-1998 13:44		

Parallel Port Header

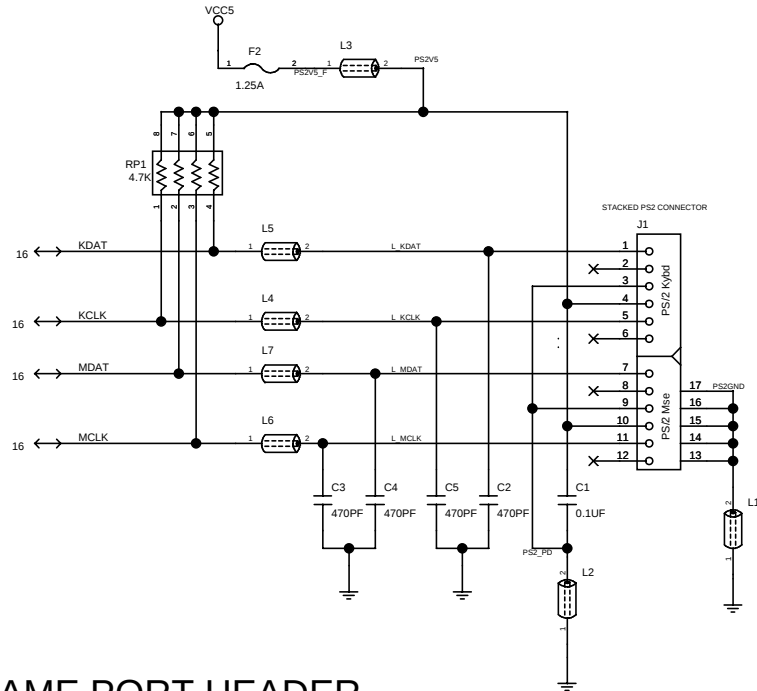


TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD		REV: 1.3
PARALLEL PORT		
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION	PROJECT: INTEL(R) 810 CHIPSET
	LAST REVISED: 2-22-1999 11:02	SHEET: 21 OF 40

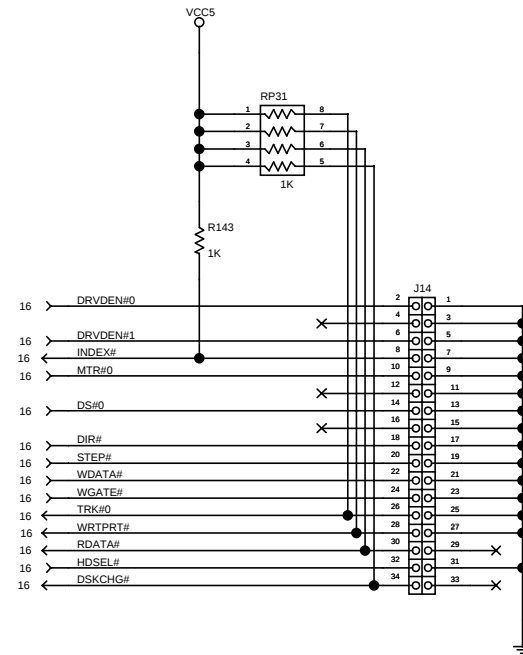
Serial Port/COM Headers



KEYBOARD/MOUSE PORTS

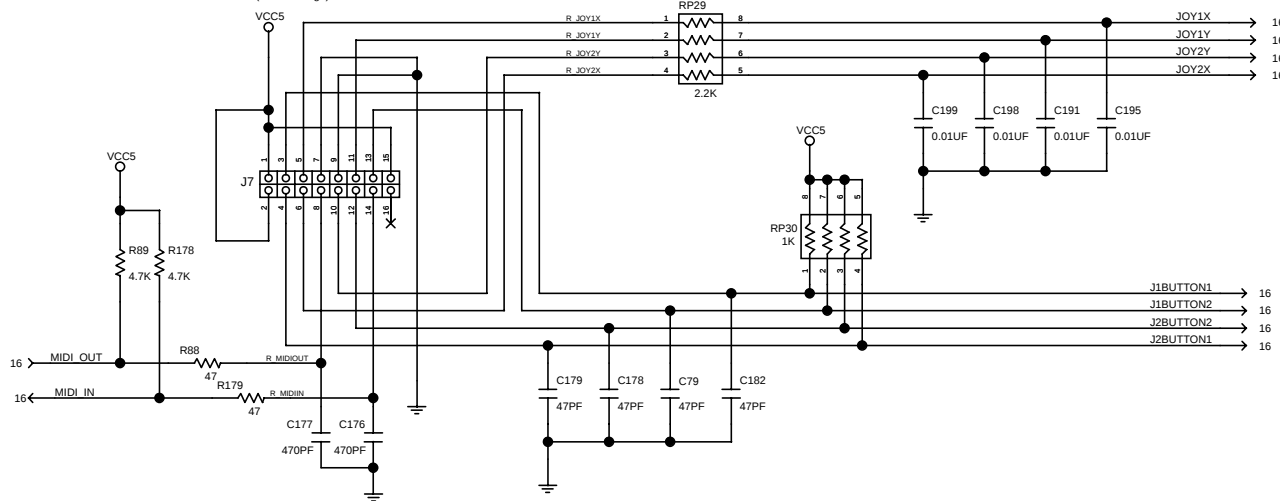


FLOPPY DISK HEADER



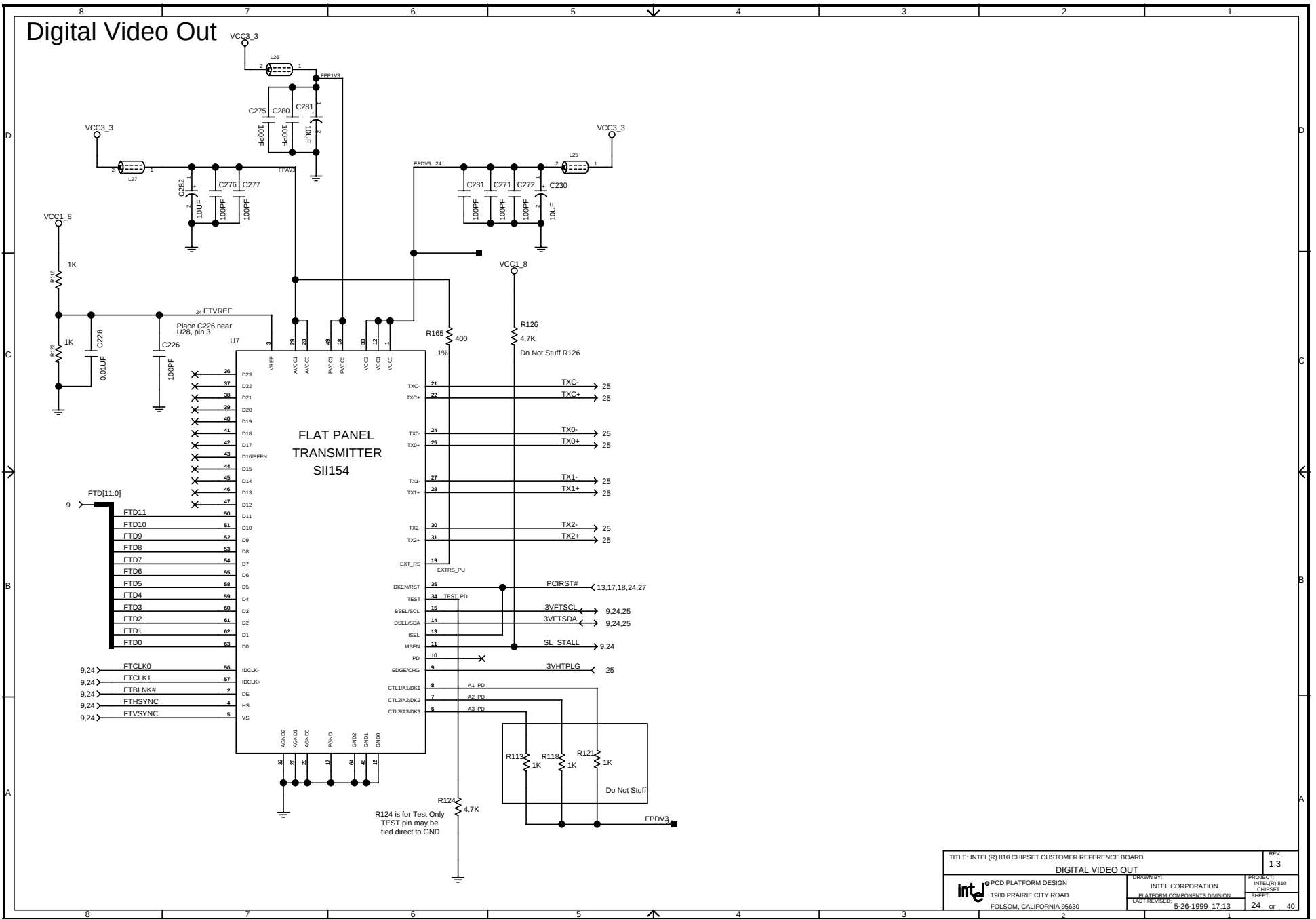
GAME PORT HEADER

J7 Pinned Out for IDC (Flow Through) Ribbon Cable Connector



TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD			REV: 1.3
KEYBOARD/MOUSE/FLOPPYGAME PORTS			
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY:	INTEL CORPORATION	
	LAST REVISED:	PLATFORM COMPONENTS DIVISION	
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		23 OF 40	

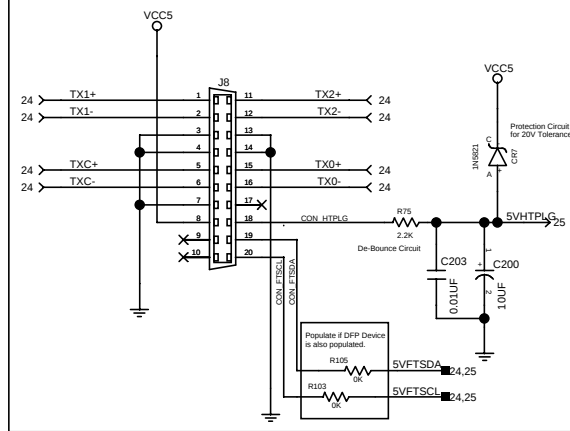
Digital Video Out



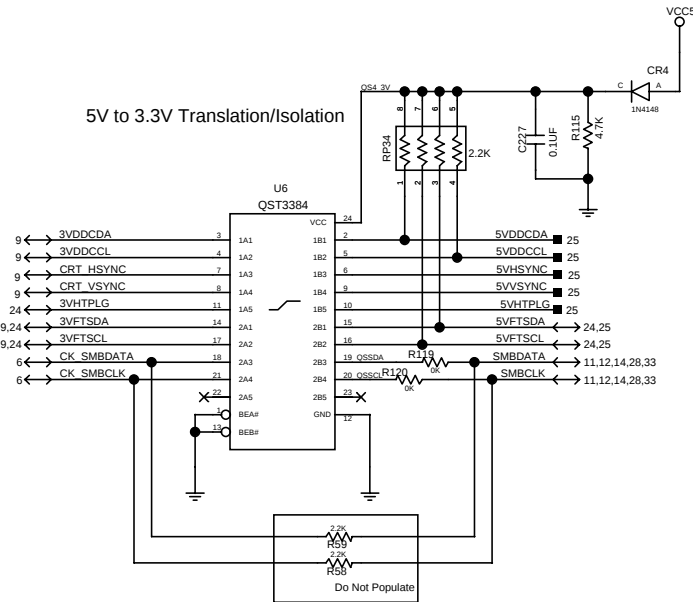
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DIGITAL VIDEO OUT			
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION		PROJECT: INTEL(R) 810 CHIPSET
	PLATFORM COMPONENTS DIVISION		SHEET
	LAST REVISED: 5-26-1999 17:13		24 OF 40

Video Connectors

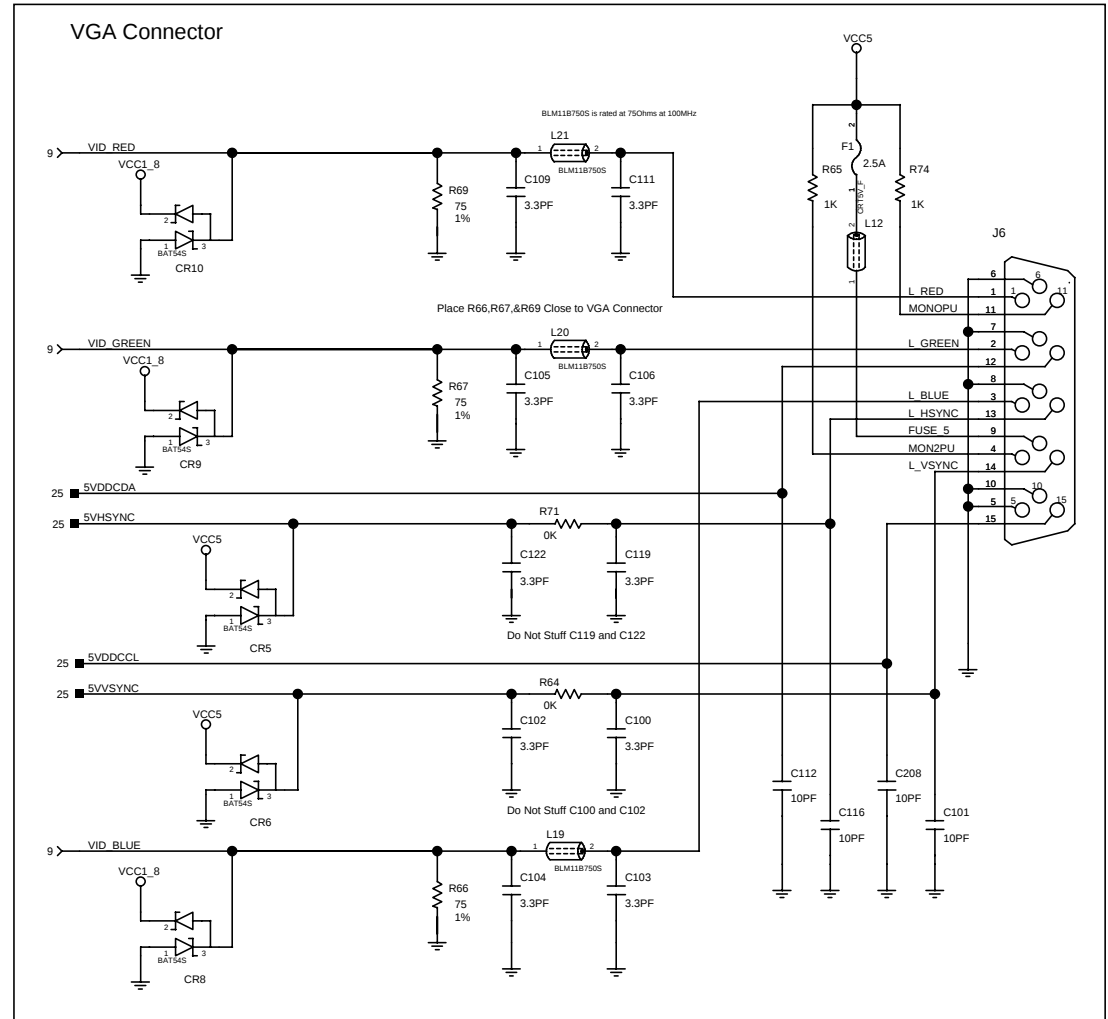
20 Pin Flat Panel Connector



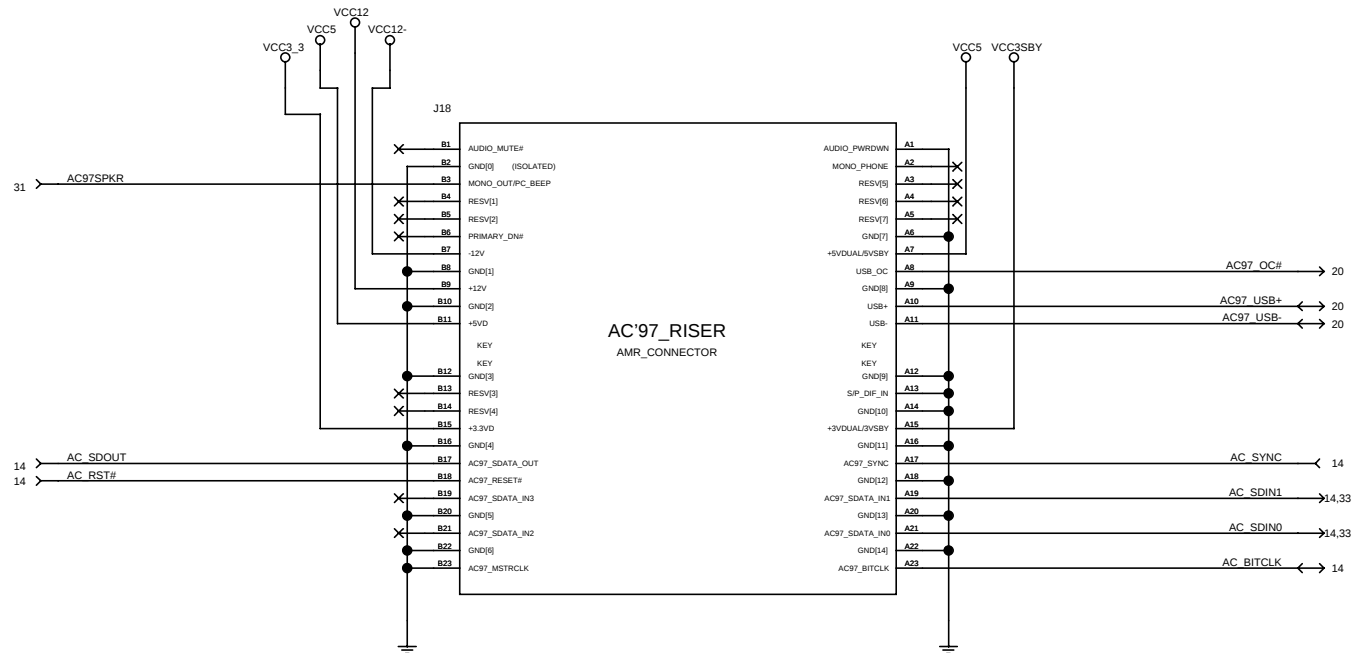
5V to 3.3V Translation/Isolation

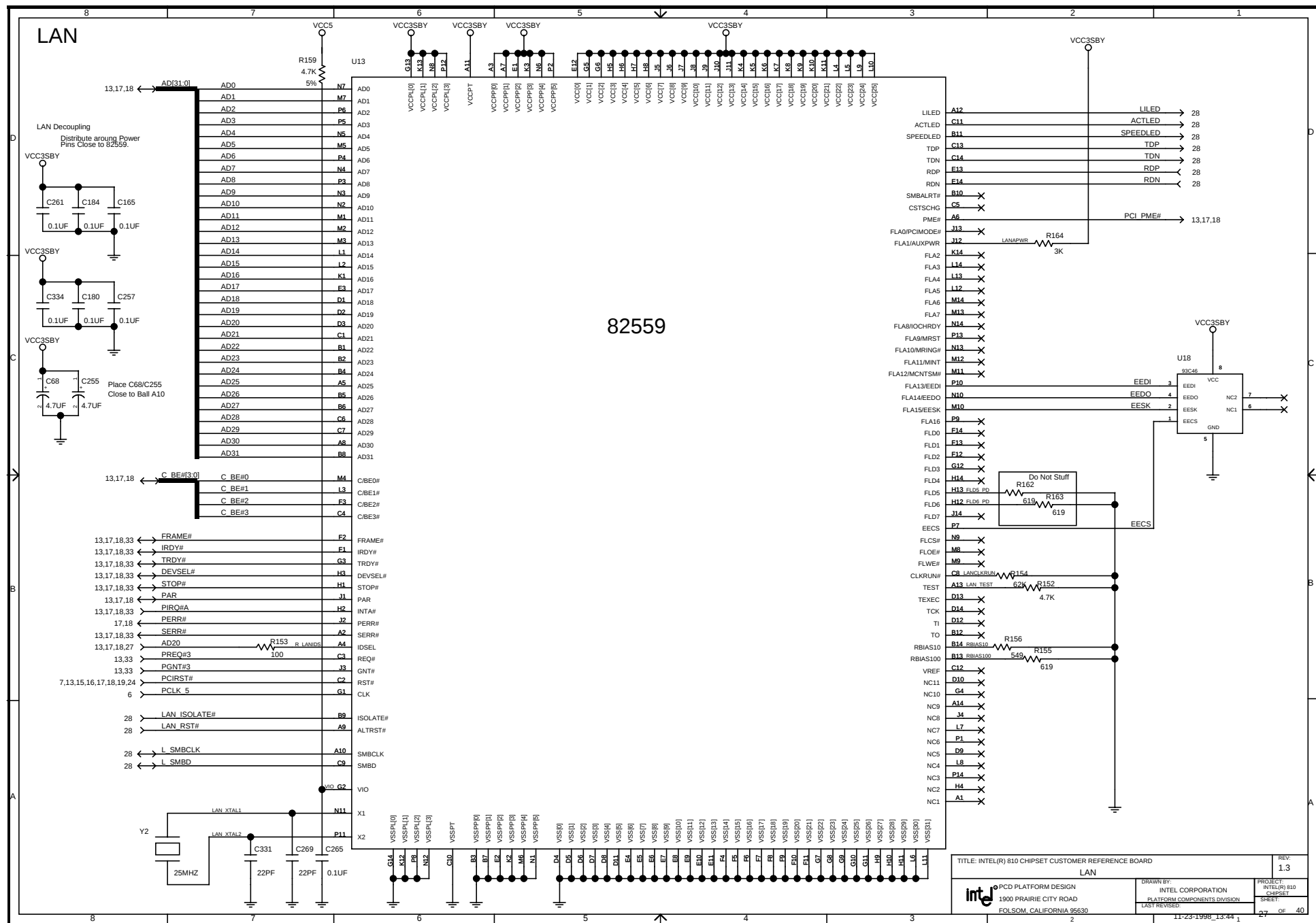


VGA Connector

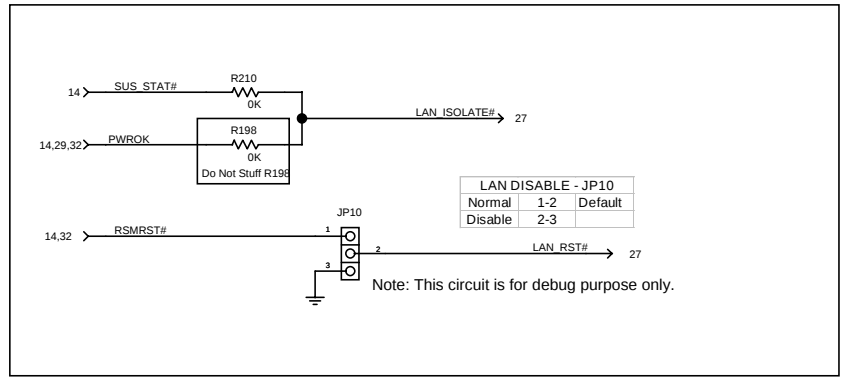
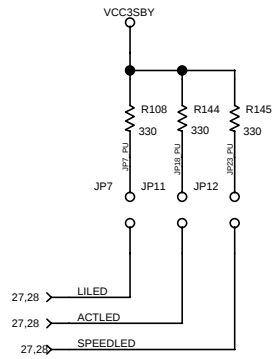
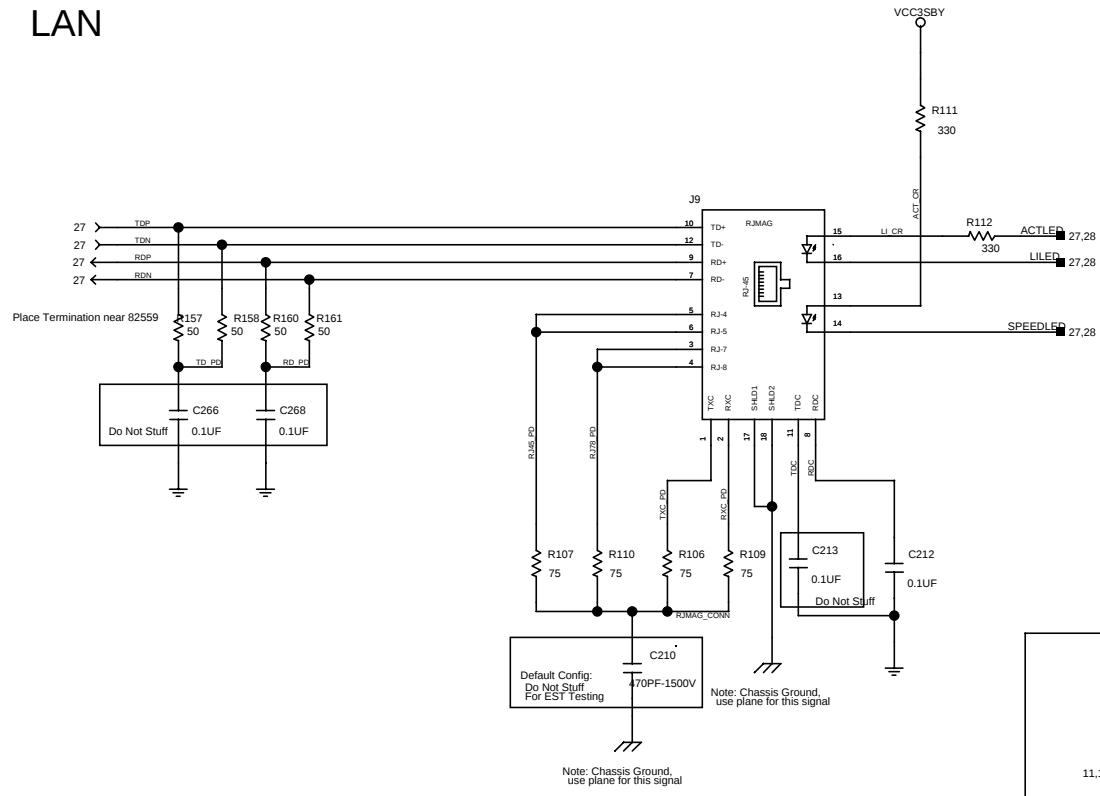


AUDIO/MODEM RISER

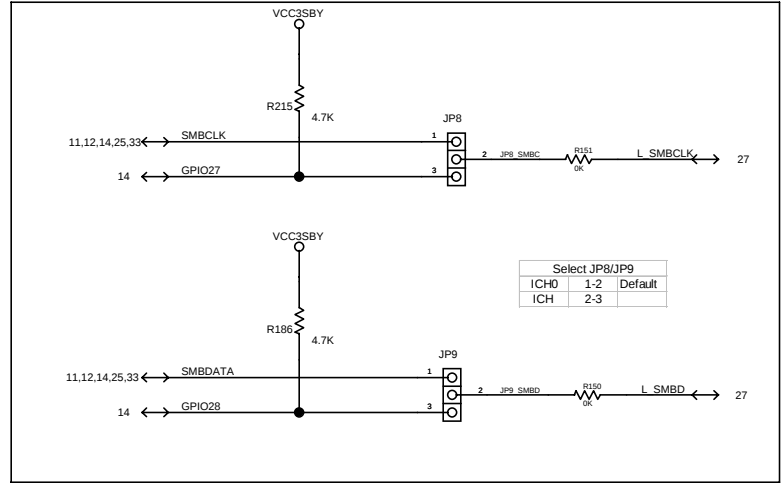




LAN



LAN DISABLE - JP10		
Normal	1-2	Default
Disable	2-3	

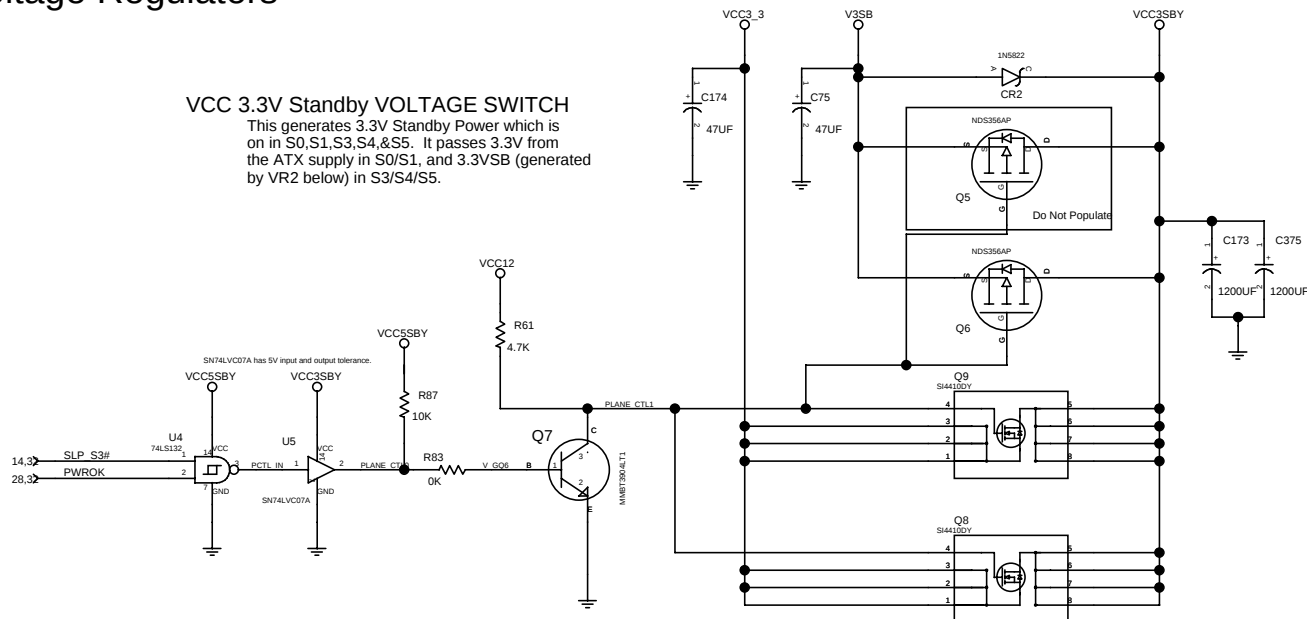


Select JP8/JP9		
ICH0	1-2	Default
ICH	2-3	

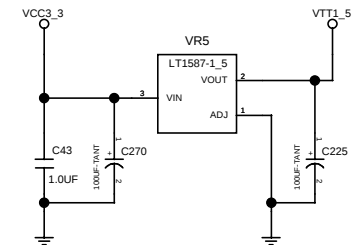
Voltage Regulators

VCC 3.3V Standby VOLTAGE SWITCH

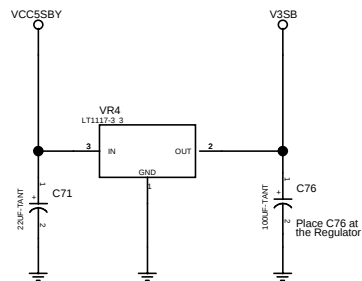
This generates 3.3V Standby Power which is on in S0,S1,S3,S4,&S5. It passes 3.3V from the ATX supply in S0/S1, and 3.3VSB (generated by VR2 below) in S3/S4/S5.



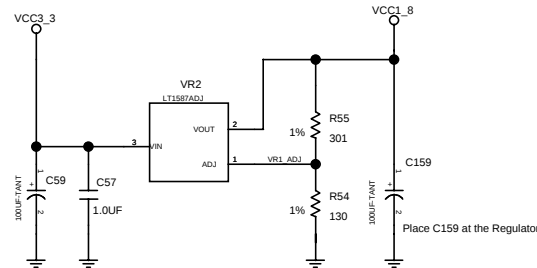
VTT 1.5V VOLTAGE REGULATOR



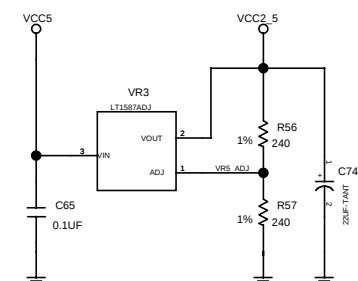
VCC 3.3VSB Regulator



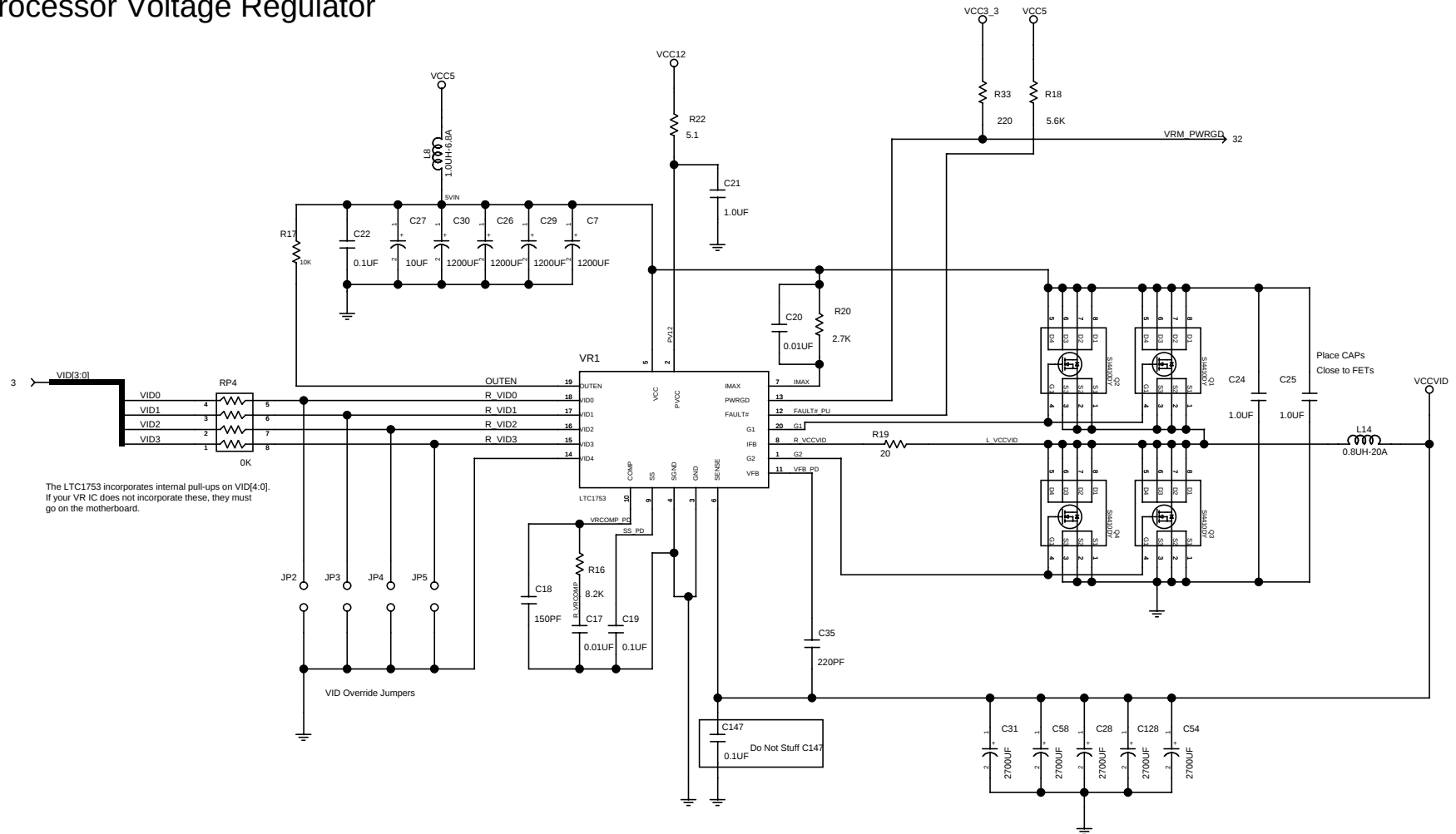
VCC 1.8 VOLTAGE REGULATOR



VCC 2.5 VOLTAGE REGULATOR

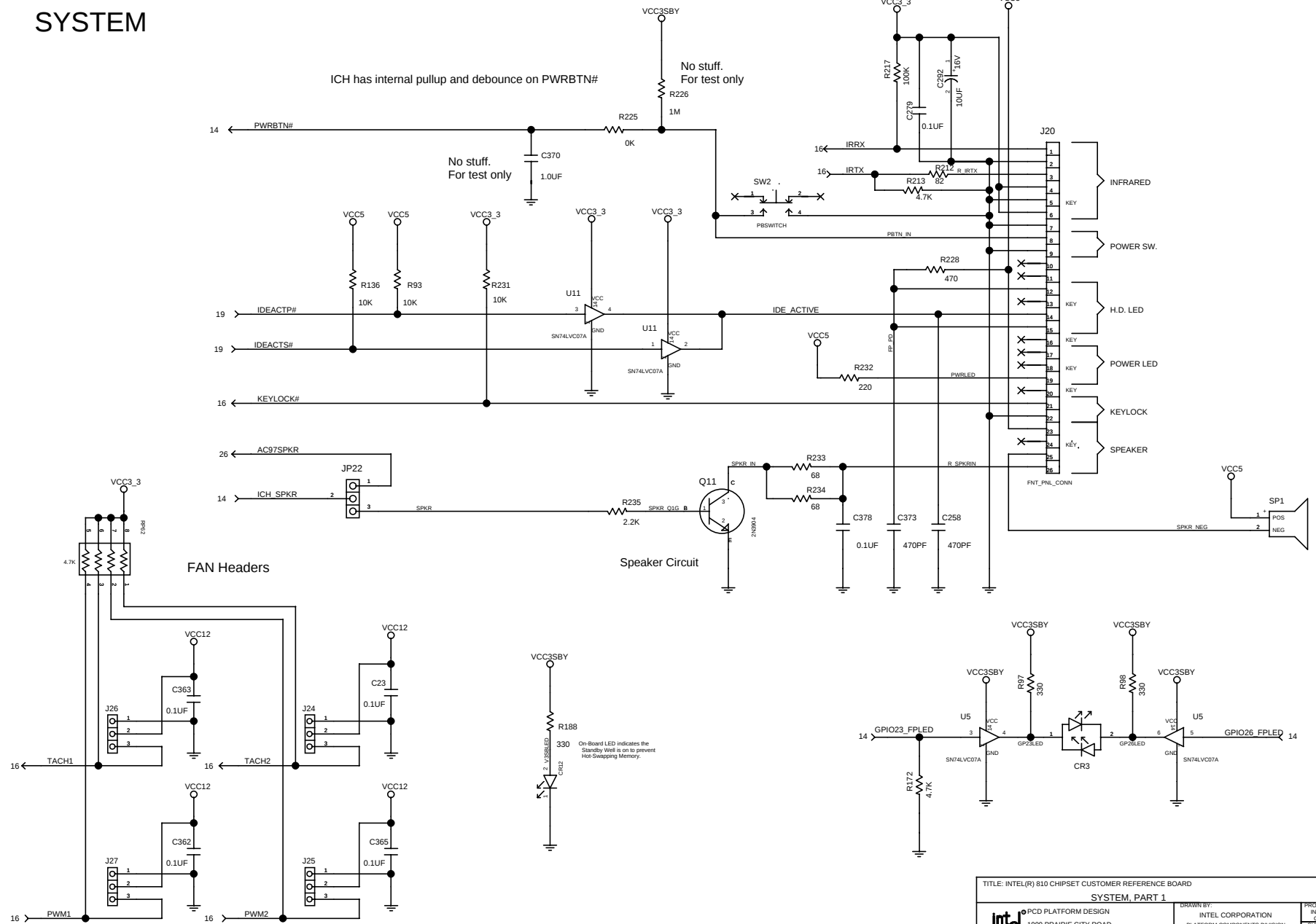


Processor Voltage Regulator



Refer to VR Supplier for Layout Guidelines

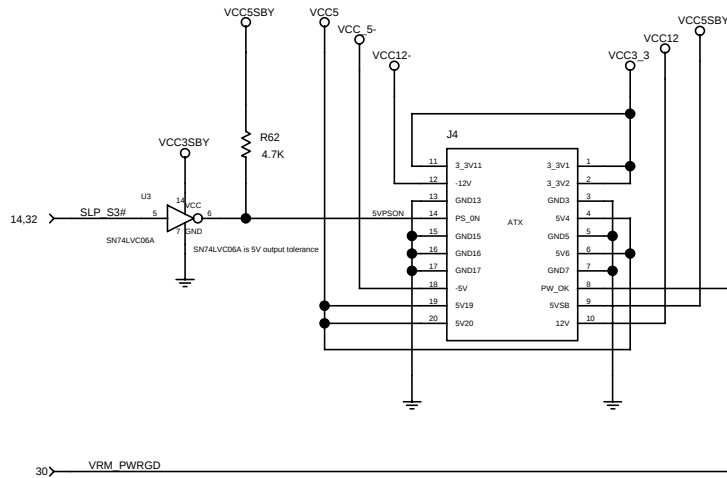
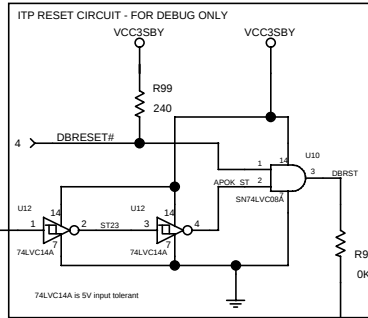
SYSTEM



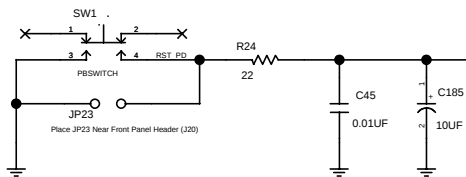
SYSTEM

Power Connector and Reset Control

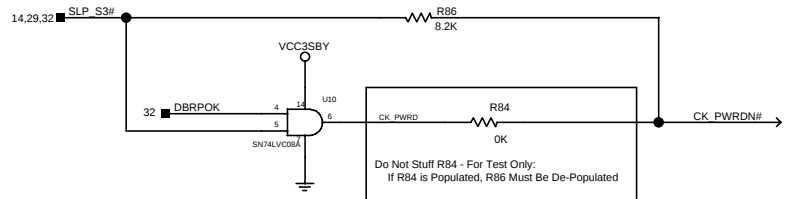
Power Good Circuit



Reset Button

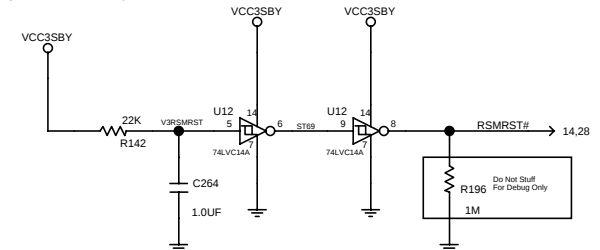


CLOCK POWERDOWN CONTROL



Resume Reset Circuitry

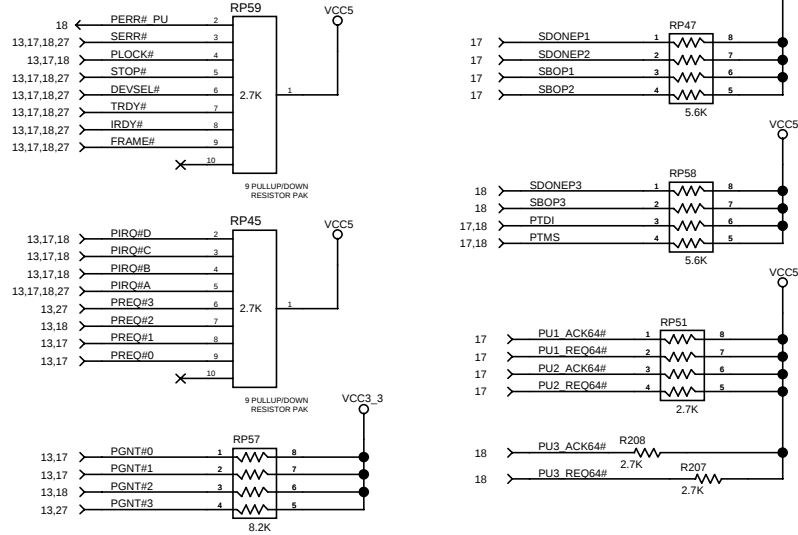
Schmitt Trigger Logic
using a 22msec delay



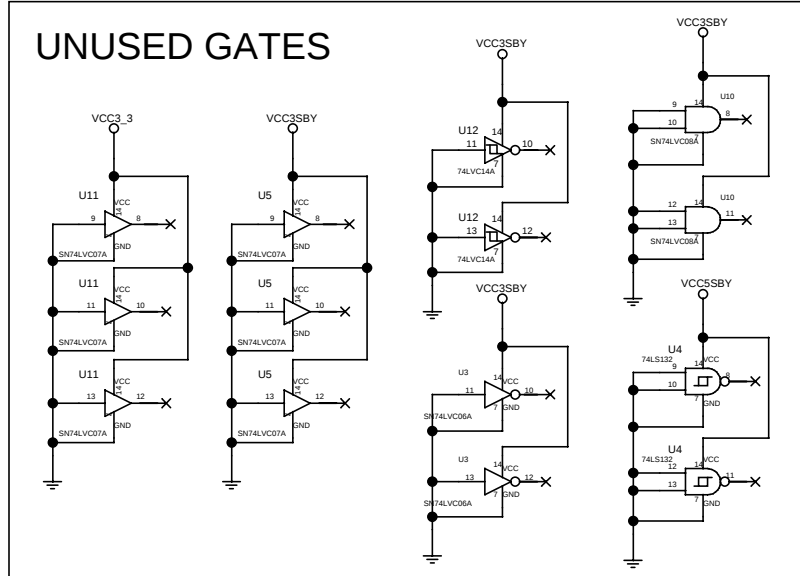
TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD			REV: 1.3
SYSTEM, PART 2			
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION	PROJECT: INTEL(R) 810 CHIPSET	
	LAST REVISED: 12-6-1998 12:54	SHEET: 32 OF 40	

PULL-UP RESISTORS AND UNUSED GATES

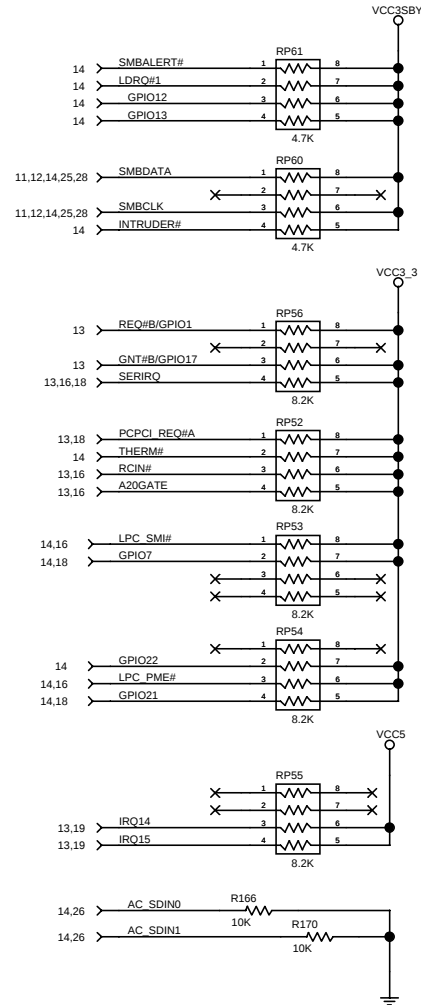
PCI BUS



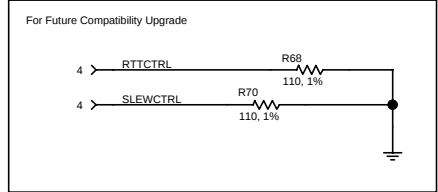
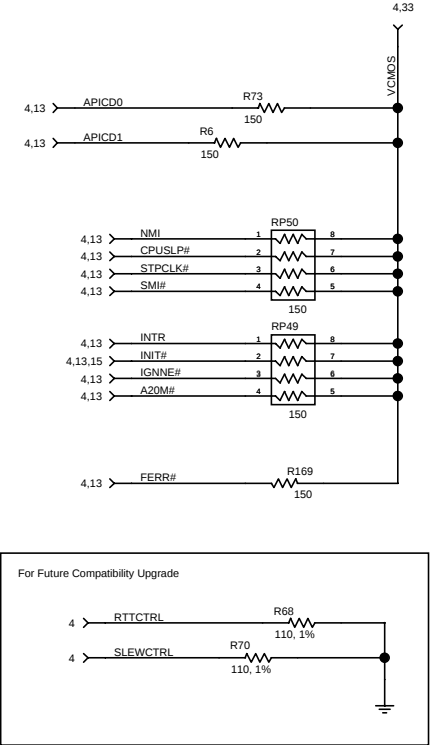
UNUSED GATES



ICH0



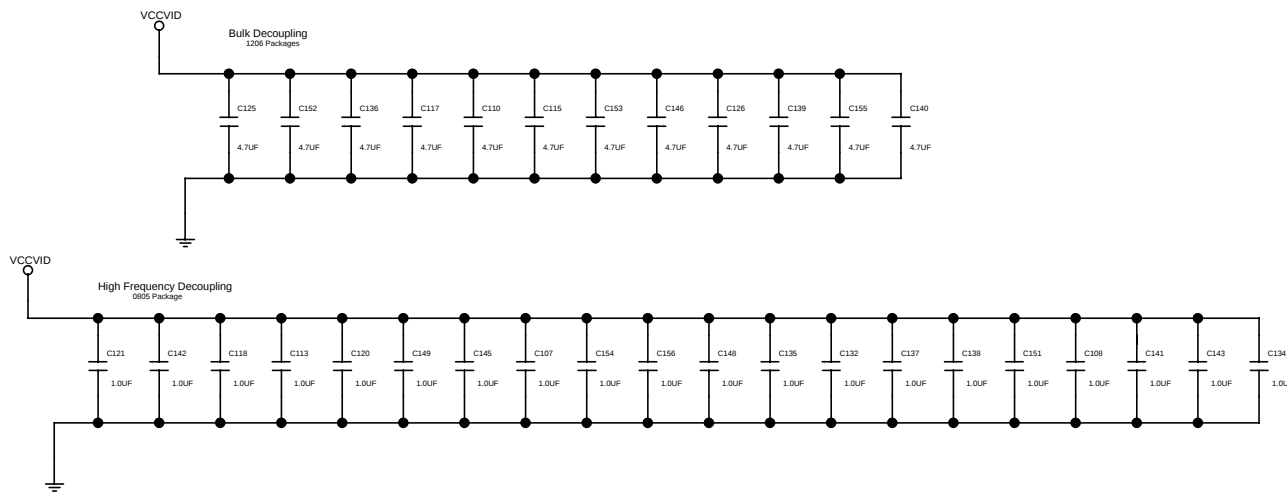
CPU



370-pin Socket Decoupling

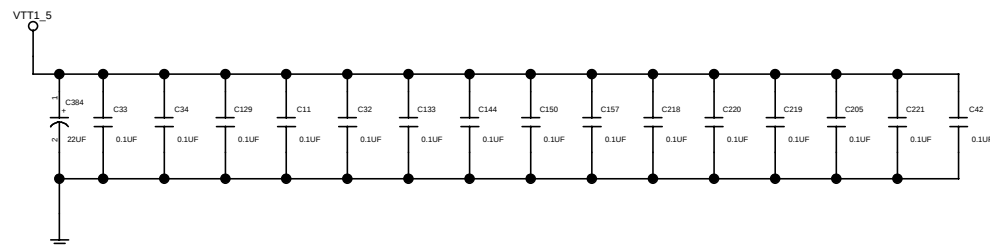
VCCVID Decoupling

Place in 370 PGA Socket Cavity



VTT Decoupling

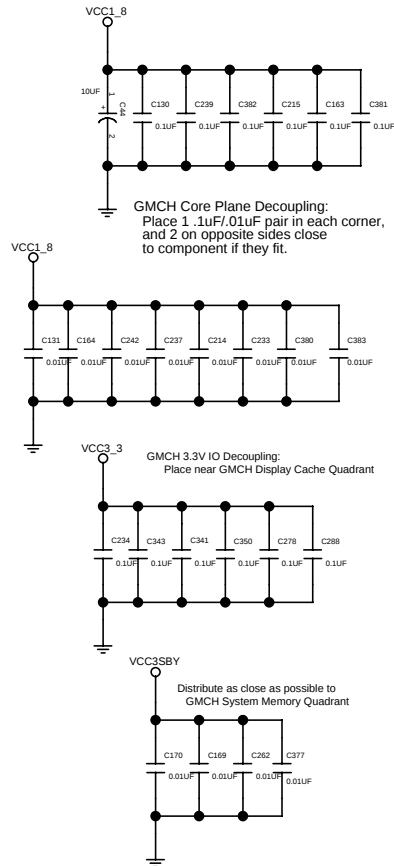
0805 Package placed within 200mils of VTT Termination R-packs
One Capacitor for every 2 R-Packs



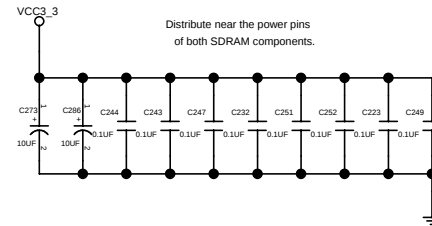
TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD			REV: 1.3
VRM DECOUPLING			
PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION	PROJECT: INTEL(R) 810 CHIPSET	
	LAST REVISED: 12-8-1998 14:04	SHEET 34 OF 40	
	PLATFORM COMPONENTS DIVISION		

DRAM, CHIPSET, and BULK POWER DECOUPLING

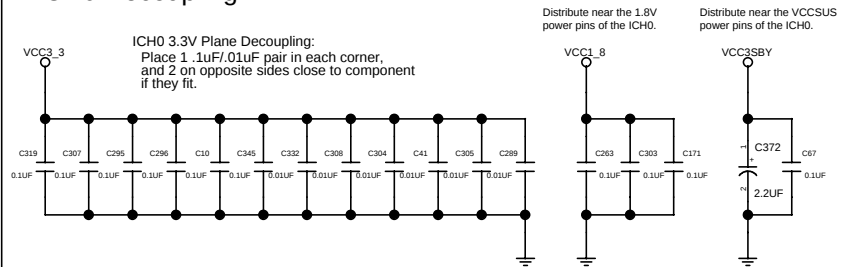
GMCH Decoupling



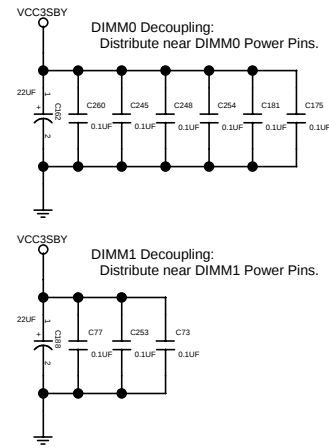
Display Cache Decoupling



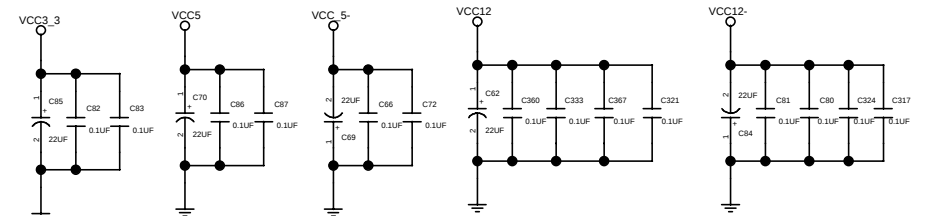
ICH0 Decoupling



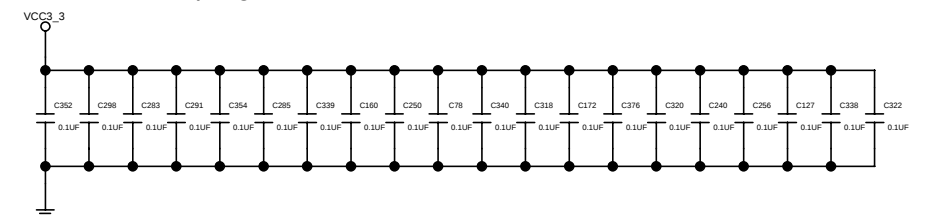
System Memory Decoupling



Bulk Power Decoupling



3 VOLT Decoupling



Revision History (Changes from Rev 0.7)

Sheet	Description	Sheet	Description
ALL	Cosmetic changes to all pages (Re-names nets, re-organized symbol arrangement, etc.)	10	Ganged the two CKEs off of one 4.7K Pull-Up to 3.3V.
4	Changed FB1 (ferrite bead for PLL analog isolation) to Inductor L2.	11	Fixed Symbol Pinout
	Changed value of R36 to 10 ohms.	12	Fixed Symbol Pinout
	Replaced R21-R23 with 1K R-pack (RP50). Replaced R24-26 and R34 with RP44.		Removed SMBUS pullups from this page. There are pullups on page 32.
	Changed R184 value to 220 ohms		Removed Reset Straps from MD lines.
	Changed Pull-Up/Down Resistor Values on signals to ITP interface and grouped into Rpacks/Discretes to make true populate/de-populate Mfg. Option.	13	Updated Ballout
	Floated THERMTRIP# Signal		Changed C172 to 0.1uF Cap (HUBREF decoupling)
	Generate GTLREF with 1% resistors. Move from page 5 to page 4.		Added Resistor Site to Pull F16 to GND for test/debug.
	Changed BR0# Pull-Down to 56Ohm to use existing GTL Term Rpack Slot on sheet 5	14	Updated Ballout
	Added Jumper Test Option to GND BSEL line.		Routed PME# and SM# to GPIO[13:12] respectively to support wake events from S1.
	Change R35 from 51Ohm, 1% to 51Ohm, 5%		Pull RTCRST# signal from input node of first RC delay rather than output node (just other side of diode).
	Added VCMOS Decoupling		Moved Clear CMOS to RTCRST# signal and Added 1K resistor to GND on pin 3 of jumper.
6	Changed VDDA (pin22) of CK-Whitney to 3.3V Supply per 0.5 Spec.		Change RTC Circuit to power Vbias straight from positive terminal of battery (BAT1). Was charged from VCCRTC input.
	Added/Modified Decoupling and Power Isolation		Changed AC_SYNC pull-down strap (CPU Safe Mode Jumper JP14) to AC_SDOUT pull-up strap.
	Ganged CPU and GMCH Clock Lines		Change C8 and C9 to 12pF caps.
	Isolated USB/DotCLK power (pin 27) from SDRAM power		Tied OC#0 and OC#1 together.
	Changed PowerDown control signal to NAND of SLP_S3# and PWR_OK		Add jumper straps to SPKR and AC_SYNC
	Change C146 and C147 from 10pF to 12pF		Remove Pull-up from SLP_S3# signal
7	Updated GMCH Ballout	15	Updated FWH pinout and labelled symbol as a TSOP Socket.
	Changed GTLREF divider to 1% resistors and GTLREF Decoupling to a 0.1uF (C2) and 0.001uF (C72) in parallel		Updated FWH (Socket) Symbol to include FGPI[4:0], routed ATA66 cable detect to GPI[1:0] and pulled rest down through 8.2K.
8	Updated GMCH Ballout		Combined Decoupling Caps and reduced to appropriate amount.
	HUBREF Generated from two 1% resistors with 0.1uF (C171) at GMCH HUBREF pin.		Changed JP4 to a 2 pole instead of 3 pole jumper.
	Changed C3 to 20pF Cap		Replace discrete resistors with R-packs. Replaced R84-87 with RP42.
	Decoupled System Memory 3.3V balls from Local Memory 3.3V balls. System Memory quadrant connects to 3.3Vsb plane and Local Memory connects to 3.3V plane.	16	Updated Pinout. Connected new VREF pin to 5V.
9	Updated GMCH Ballout		Added Decoupling to IRRX/IRTX lines.
	Connected VCCDACA and VCCDA signals to 1.8V through filtering circuitry. Connected VSSDACA and VSSDA to Digital GND.		Routed PME# and SM# to GPIO[13:12] respectively to support wake events from S1.
	Added Reset Strap jumpers to LMD[31:26].		Routed Game Port to game port header, 2nd Serial Port to serial header, PWM/Tach signals to fan headers, and unused signals to test header.
	Added Oscillator to DotCLK for Test/Debug option		Routed Unused GPIOs signals to test header.
	Connected Digital Video Out signals		Removed JP6 and Grounded CLOCKI.
	Changed R70 to 330hm and C4 to 20pF.		Connected VTR to VCC3.3 (removed from VCC3SB well) and added power decoupling.
			Pulled SYSOPT pin down to GND through 4.7K resistor.
			Moved Keylock pull-up sheet 31.

Revision History (Changes from Rev 0.7)

Sheet	Description	Sheet	Description
17	Changed device numbers (IDSEL wiring) for slots to AD16, AD17, and AD22. Routed additional signals required to AD22 slot to support ISA bridge test card.	27	Changed 93C46 Pinout.
18	Changed device numbers (IDSEL wiring) for slots to AD16, AD17, and AD22. Routed additional signals through 0K resistors to AD22 slot to support ISA bridge test card.	28	Replaced RJ45 connector and discrete magnetics with integrated RJ45/magnetics part and connected accordingly.
	Added Jumper to route PERR# to ICH/ICH0 if ICH is populated.		Added LAN Disable Jumper.
19	Connected pin 34 of each connector to P66DETECT and S66DETECT(FWH_GPI0 and FWH_GPI1 respectively).		Added ICH/ICH0 scalability jumpers.
	Buffered PCIRST# signal going to pin 1 of IDE connectors to isolate cable loading.	29	Moved Power Connector to Sheet 32
	Removed Series Terminations from IRQ lines (pulled into ICH0).		Replaced old VCC5dual circuit, with VCC3Sby Circuit which generates supply for devices which must stay powered in S3. Removed LT1585-3.3 (U36 on rev0.7).
20	Isolated each VCC input to USB stacked connector through dedicated filtering circuitry.		Changed U27 from LT1585-1.5 to LT1587-1.5 and changed discretes.
	Added 47pF EMI caps on USB data lines.		Added V3SB regulator (generated V3SB from V5SB from ATX power supply).
	Connect USB through Audio/Modem Riser through 0K resistors.		Changed 1.8V Regulator design from LT1585ADJ to LT1587ADJ and changed discretes.
	Make OC detect circuitry unique to each port and update polyfuse value.		Changed 2.5V Regulator design from LT1585ADJ to LT1587ADJ and changed discretes.
21	Replaced DB25 connector with 2x13 header so we can cable out. SMB	30	Added VRM Override Jumpers to VID bus.
	Removed Series Termination Resistors from Ack# and Busy# signals.		Change VR Design to VRM8.4 compliant design. Use LTC1753 per Linear App Note.
	Changed Pull-ups to 2.2K	31	Moved Reset and Power circuitry to sheet 32
22	Added 2nd serial port and connected both through 2x5 headers to cable out (Removed 1 DB9 Connector).		Added Infrared, Power Switch, Hard Drive/Power LEDs, Keylock, and Speaker Circuitry to Common System Header.
	Added discrete solution to level translate and route Ring Indicate from Serial ports to ICH for Wake from S3 on serial modem.		Added 12V Fan Headers (2 supporting TACH outputs, and 2 support PWM inputs).
23	Added MIDI/Game Port circuitry connected through 2x8 header to cable out.		Added Debug LED to monitor 3.3VSBY Plane
	Increased Cap values on Keybd/Mouse lines from 100pF to 470pF.	32	Moved Pull-ups to sheet 33.
	Changed the keyboard and mouse symbols to a PS/2 stacked connector.	32	Updated new PWROK/PWRGOOD Generation, RESET, RSMRST# circuitry.
25	Changed RGB PI filter caps from 22pF to 3.3pF.	33	Pulled-Up SMBUS interface to 3.3VSBY instead of 3.3V.
	Added Quick Switch to level translate the CRT Sync, CRT DDC, and Flat Panel DDC Signals.		Removed R164 (FLUSH#) and R168 (THERMTRIP#) pull-ups. Removed pull-up on PWRGOOD (pulled up on sheet 32). Grouped remaining pull-ups to 1 1K Rpack.
	Isolated CK-Whitney from SMBUS in Power Down through Voltage translation Quick Switch.		Changed all PCI 3.3V pull-ups to 8.2K per PCI spec.
	Changed VGA Connector symbol.		Combined like pullups into R-packs where possible.
	Added EMI Caps on SYNC and DDC Signals.		Added 8.2K pull-ups to SERIRQ and ICH0 unused GPIOs.
26	Routed USB up the AMR Connector.		Added Pull-Up Sites for FLUSH# and 370PGA Socket Pin W35 to VCMOS for future compatibility upgrade.
	Ran 5V (instead of 5VSB) to Audio Modem Riser.	34	Updated Processor Decoupling per latest Guidelines for 370PGA socket.
	Added stuffing option AC'97 debug port	35	Added System Decoupling

TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD		REV: 1.3
REVISION HISTORY, PART 2		
 PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION LAST REVISED: 11-23-1998 13:43	PROJECT: INTEL(R) 810 CHIPSET SHEET: 37 OF 40

Revision History (Changes from Rev0.9 to Rev0.95)

Sheet	Description	Sheet	Description
2	Changed "Video Encoder" box on Block Diagram to "Digital Video Out Device" Box. Added Device Table	20	Changed R117,R118,R121,R122 from 27ohm to 15ohm-1% Resistors
3	Changed Reference Designator on 370-pin Socket from J20 to X1	22	Change R207 from 47K to 10K
4	Changed Reference Designator on 370-pin Socket from J20 to X1 Changed C1 from 22uF,30% to 47uF,10%	23	Moved RP31 from pg. 16 to pull-up Key/Mouse lines to filtered VCC5. Added 470pF Caps on MIDI lines (C327,C328).
6	Changed Series Termination Resistor Values from 22 Ohms to: R37,R38,R55,R56,R57=43ohm,2%; R39,R40,R41,R42,R43,R46,R47,R58,R59,R60,R61=33ohm,2%; R45,R48,R49,R50,R51,R52,R53,R54,R63=33ohm,5%; R44,R226=10ohm,5% T'ed REFCLK and added R226 (to separate termination to ICH and SIO). Renamed CLK14 to SIO_CLK14 and ICH_CLK14 for each new NET out of the T. Changed C144 and C185 from 4.7uF to 22uF.	25	Moved R67,R68,R69 from Sheet 9. Cleaned Up VGA Connector Schematic
8	Added Cap Site to GMCH Hub Clk Added 0K Resistor (R231) in series with DCLK_WR		Added Provisions to add PI Filters on VSYNC and HSYNC Lines
9	Changed Reference Designator on Oscillator Socket from U34 to X2 Corrected Connection of Debug Oscillator from DDSCDA to DOTCLK NET. Updated Pin Numbers to match GMCH 0.7 EDS Ballout Added 0K Resistor (R232) in series with LRCLK Added Cap Site to ICH Hub Clk Replace Bead FB21 with Inductor (L4) - 68nH to create LC filter (<130kHz) Added LC filter to 1.8V plane connected to balls U6 and E19. Changed Test Oscillator Circuit (U34) to remove shorted jumper and add decoupling. Changed pin names on 48MHz oscillator symbol. Moved R67,R68,R69 to Sheet 25.		Changed 5V Supply to Quick Switch to pull-down on DIODE output. Also pulled DDC lines up to the same supply powering the Quick Switch. Change R132,R133 from 8.2K to 1K Pull-Ups
14	Rename NET CLK14 to ICH_CLK14 Rename Pin L1 to VCCSUS1 and Pin N1 to VCCSUS2 Rename NET GPIO23 to GPIO23_FPLED, and NET GPIO26 to GPIO26_FPLED Routed LPC_SM# and LPC_PME# to GPIO[5:6] respectively from GPIO[12:13] respectively. Changed Value of C11 from 0.1uF to 1.0uF	26	Removed AC97 Debug Connector (J5)
15	Changed Reference Designator on U9 to X3	27	Changed R4 pull-up from 62K to 4.7K and added 0.1uF Decoupling to VIO pin (C262). Added Decoupling for LAN Power (C336-C341)
15	Added 0K RPACK(RP68) in series to GROUND on FWH ID lines for Test/Debug.	28	Change R140/R141 to 4.7K Resistors
16	Changed Pin 87 Name from RTS1#_SY SOP to RTS1# and Pin 50 name from GP27/IO_SM#/TEST to SP27/IO_SM#	29	Modified CK_PWRDWN# Generation Circuitry to pull off U33 NAND gate and invert through U13 to get correct logic level. Previously it was tapped off the base of BJT Q6. This would have kept CK_PWRDWN# from charging higher than 0.7V (drop across BE junction) Changed R191 to 10K, R192 to 0K, and R193 to 4.7K
16	Rename NET CLK14 to SIO_CLK14	30	Changed Reference Designator on U15 and U25 to Q9 and Q10 respectively. Changed Reference Designator on U8 to VR5, U11 to VR3, and U27 to VR4 Changed C268 and C259 to 1.0uF,X7R caps Added 2 more Si4410DY FETs in parallel with two there (Q7/Q8) Changed C160-C163 to 2700uF and added one more (C342) in parallel. Change C153 to 220pF Changed connections of COMP and SS to show them returning directly to SGND pin. Added Inductor (L13) to filter 5V input to VRM
16	Moved RP31 to pg. 23 to pull-up Key/Mouse lines to filtered VCC5.	31	Change reference designator S1 to SW1 Change C79 to 1.0uF
17	Swapped ACK64# and REQ64# to route to correct pins per PCI spec.		Add Front Panel Dual LED Circuit controlled by ICH GPIOs
18	Swapped ACK64# and REQ64# to route to correct pins per PCI spec. Replaced JP6 Jumper with 0K Resistor Stuffing Option (R233, R234)	32	Change ATX connector Reference Designator from U6 to J29. Change reference designator S2 to SW2
19	Inserted 0K Stuffing Resistors in Series with ATA66 Cable Detect (R235,R236)	33	Removed Pull-Ups from GPIO23/GPIO26 Pulled LDRQ#1 Up to 3.3V Sby (instead of 3.3V).
19	Swapped 74LS07 out for 74LV C07A and connected to 3.3V.		Changed PCI Pull-Up Resistor (R99,R100,RP53,RP46,RP47) values from 8.2K to 2.7K and connected to 5V. Also connected RP40 and RP43 to 5V (from 3.3V) to maintain compatibility with more 5V PCI cards. Removed RP49 (VID Pull-Ups) Since internal to LTC1753
		35	Added additional Decoupling for Various Components (C343-C389) Changed C217-C220 from 0.1uF to 0.01uF
		ALL	Changed Reference Designators on All Ferrite Beads from FB* to L*.

TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD

REV:
1.3

REVISION HISTORY, PART 3

PCD PLATFORM DESIGN
1900 PRAIRIE CITY ROAD
FOLSOM, CALIFORNIA 95630DRAWN BY:
INTEL CORPORATION
PLATFORM COMPONENTS DIVISION
LAST REVISED: 11-23-1998 13:43PROJECT:
INTEL(R) 810
CHIPSET
SHEET
38 OF 40

Revision History (Changes from Rev0.95 to Rev0.99)

Sheet	Description	Sheet	Description
4	Changed C1 to 33uF and L2 to 4.7uH.	24	Change C330 to a 100pF cap and Scaled Back Decoupling on power planes to U28..
	Connected E21 to VCC_DET Pull-Up		Swapped Connectivity of FTCLK0 and FTCLK1.
	Added 0603 Cap Site on CPUHCLK	25	Fixed Connectivity of CR2, CR4, CR5, CR6 and CR7. In all cases Pins 1 and 2 were swapped.
	Removed RP50 and routed TCK and TMS to 330ohm pull-ups in RP44.		Change L8,L9,L10 Part Number to BLM11B750S
5	Changed Rpack connections per Layout Back Annotation		Changed F3 from 2.0A Fuse to 2.5A Fuse.
6	Changed R39-R43,R46,R47,R58-R61 to 33ohm,5% (from 2%)	27	Removed Pull-up from LANTCK (U29.D14) and made No Connect. R136 moved to Sheet 16 to Pull-up LPCPD (U16.27).
	Routed CK_PWRDN# to Clock Chip (SLP_S3# thru 8.2K resistor by default).		Removed C338,C339,C340,C341 and Changed C336,C337 to 4.7uF Polarized Capacitors.
7	Added 0603 Cap Site on GMCHHCLK		Changed INTA# (U29.H2) from PIRQ#D to PIRQ#A and Changed LAN IDSEL (R142.1) from AD19 to AD20.
8	Changed HUBREF Voltage Divider Resistor Values (R182 and R185) from 1K-1% to 301ohm-1% and added AC Decoupling Discrete Sites (C394,C395,R245,R246)	28	Made C74 a 470pF-1500V cap and added "For EST Testing" Note.
9	Added 22ohm series term (R242) to LTCLK Net (U22.K22).		Changed J28.14 connection from ACTLED to SPEEDLED and Changed R219.1 connection from VCC3SBY to ACTLED
	Moved C323, C324 to page 34 and made C324 0.01uF.		Added Provision for Isolating 82559 either on SUS_STAT# or PWROK
	Removed L5 and C325. Change C5 to 33uF. Connect U22.U6 and U22.E19 direct to VCC1_8 Plane. Change U22.AB21 and U22.AB23 to connect to VCC1_8.	29	Changed Reference Designator U14 to Q10 and U16 to Q11.
	Removed Series Terms on Digital Video Out Port		Renamed NET CK_PWRD to IN_U5, and Deleted connection to U13 pin 9
	Added 0K (R31) in series with Debug Oscillator		Removed CK_PWRDWN# NET, R240
	Routed DC_MD27 (core detect Strap) to 10K to 220 pull-up on VCCDET net.	30	Connected Q4.{5-8}/Q7.{5-8}, C193, R150 to Net 5VIN instead of direct to VCC5.
14	Changed C148 from 2.2uF Monolithic to 2.2uF Polarized		Added 0K Rpack (RP69) in Series to VID[3:0] pins of VR3.
	Changed Reference Designator on BAT1 to X4 (it is a socket footprint).	31	Changed Switch Symbol to 4-pin device to match physical device.
16	Pulled Up SUSSTAT to 3.3V through 4.7K (R136, which was removed from LAN page) resistor and disconnected from ICH0.	32	Changed RefDes U6 to J29.
19	Changes to P66DETECT and S66DETECT NETs to support both Drive and Host Sided 80 conductor cable detection: Added C392 and C393 (0.047uF, X7R, 16V, 10%) to GND, 0ohm Resistors in Series (R235,R236), and 15K Pull-downs (R243,R244) to GND.		Changed Switch Symbol to 4-pin device to match physical device.
20	Fixed Connectivity of Resistor R124. USBV5 Net now Connects directly to L26 terminal 1, and R124 disconnected from L26 terminal 1. Eliminated unwanted resistor divider on 5V power pins at USB port.		Added provision for sending early powerok to Clock PD# pin for clean Power-up
	Added Series Resistors (0K) to decouple ICH USB signals from stacked connector if routed up AMR connector.	33	Swapped SIP Rpacks on CPU and ICH pull-ups to 4-Element Rpacks per Layout Back Annotation
22	Changed Net Name G_ICHR# to ICHRI#_C		Change RP48 from 1K Rpack to 330ohm Rpack, and R202, and R203 from 1K resistors to 330ohm resistors for future upgrade compatibility.
		35	Added Additional Decoupling on VCC12- and VCC12

Revision History: Changes from Rev0.99 and On

Changes from Rev0.99 to Rev1.0

- Back Annotated from Layout (Reference Designator Changes/Rpack Routing Swaps)
- Changed Series Term Values on CPU and APIC Clocks to 33ohm (Sheet 6)
- Changed Series Term Values on Memory, Hub, and DOT Clocks to 22ohm (Sheet 6)
- Added 10K Pull-Ups on SLP_S3# and SLP_S5# (Sheet 14)
- Added 2 1200uF Caps on VCC3_3SBY Plane (Sheet 29)

Changes from Rev1.0 to Rev1.1

- Removed X1, R77, R78, R79 (Debug Oscillator Socket) from Sheet 9
- Connected C377 to VCC3_3SBY Plane
- Corrected Pinout of 2x5 Com Port Headers (Sheet 22)
- Added 2x1 Header (JP23) to sheet 32 for Chasses Reset Button

Changes from Rev1.1 to Rev1.2

- Added RP70 and RP71 to Sheet 8 (SM_MA Series Terms)
- Removed 330Ohm Pull-Ups from FLUSH# and TestHi (W35 on 370-Pin Socket)
- Added 110Ohm, 1% Pull-Downs to pins S35 and E27 of 370-pin Socket (RTTCTRL and SLEWCTRL)
- Changed C347 from a 2200pF Cap to a 0.047uF Cap

Changes from Rev1.2 to Rev1.3

- Changed VCCDET Net name to VCOREDET
- Changed Value of R125 to 174ohm, 1% (from 178ohm, 1%)
- Changed value of C347 back to 2200pF Cap (from 0.047uF Cap)
- Designated R126 as No Stuff per Sil 154 Specification
- Removed R123 pull-up and connected Sil154 pin 13 to reset.
- Changed RP50, RP49, and R169 from 330ohm to 150ohm

TITLE: INTEL(R) 810 CHIPSET CUSTOMER REFERENCE BOARD REVISION HISTORY, PART 5		REV: 1.3
 PCD PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: INTEL CORPORATION PLATFORM COMPONENTS DIVISION	PROJECT: INTEL(R) 810 CHIPSET
	LAST REVISED: 5-26-1999 17:09	SHEET 40 OF 38

